Nanoelectronics
Miniaturisation in Electronics:
Scaling Challenges

With slides from:

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CMOS Scaling

- Microprocessor performance: 2011 vs 1971
- Semiconductor Industry Overview (ITRS)
  - International Technology Roadmap for Semiconductors (2011 Edition)

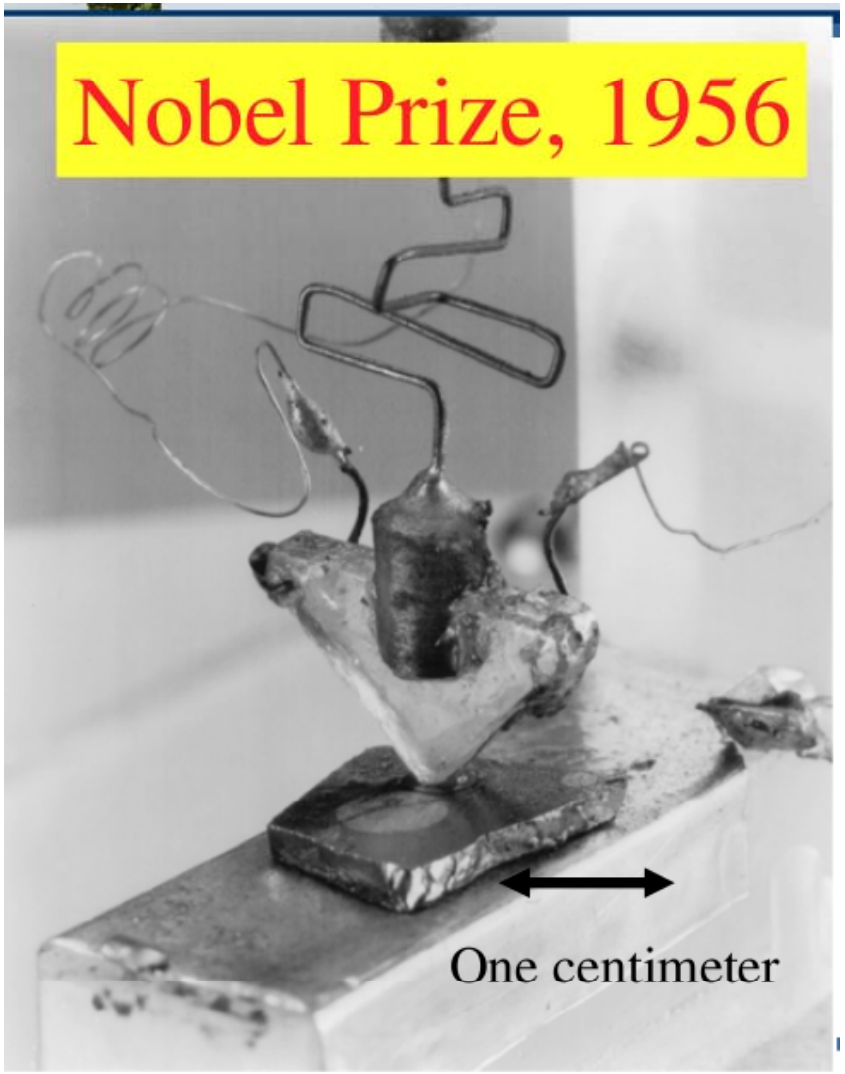
    http://www.itrs.net/Links/2011ITRS/Home2011.htm (pub. Feb. 2012)

    Executive Summary, Lithography, Emerging Research Devices, Emerging Research Materials sections

- Moore's Law (Scaling).

- Silicon Process Scaling Challenges.
  - Lithography
  - Transistor
  - Gate Dielectric
  - Interconnects
  - Power Dissipation

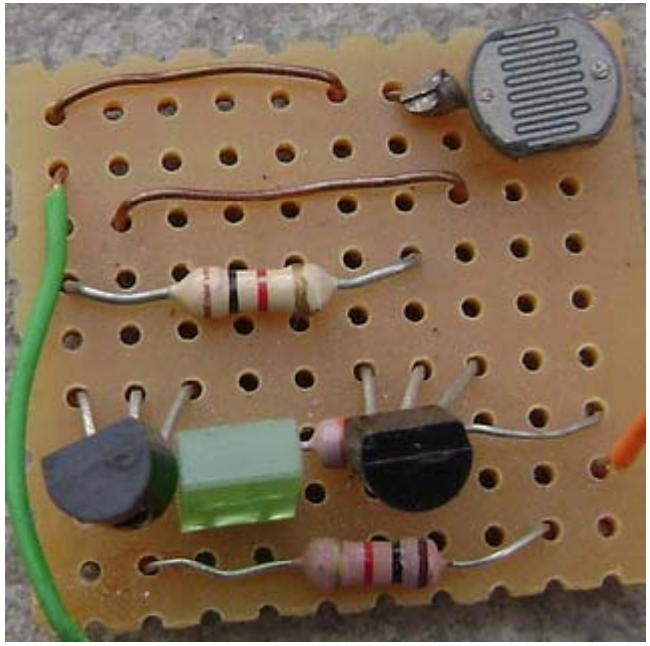
First Transistor (1947)

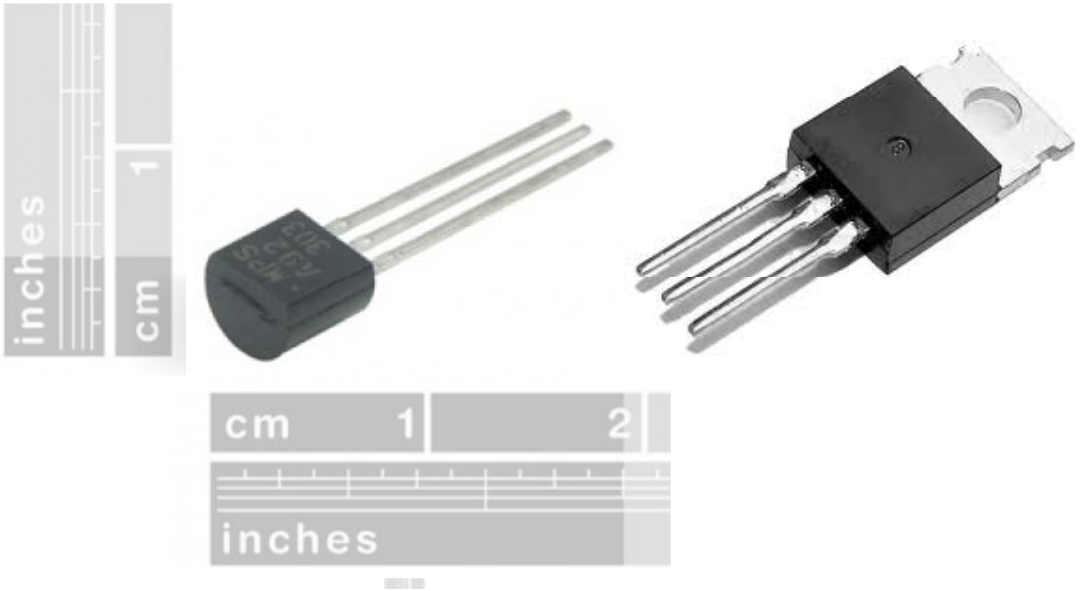


Transistor
"Transforming resistor"

At Bell laboratories in 1947

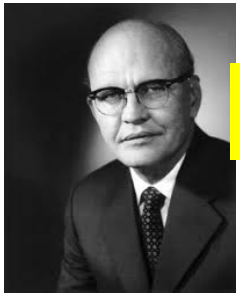
Discrete Electronic Circuits





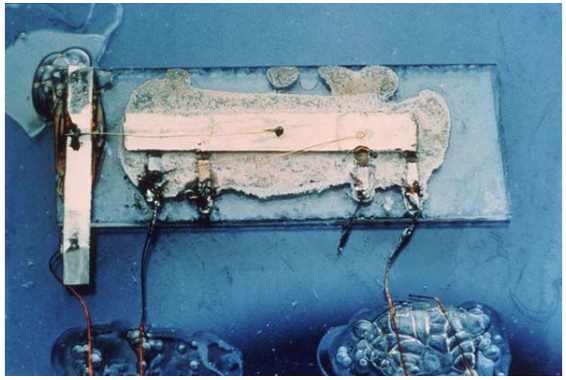
- ✓ **Electronic elements wired or soldered together onto circuit boards.**
- ✓ **Large space**
- ✓ **Expensive**

Early Integrated Circuits

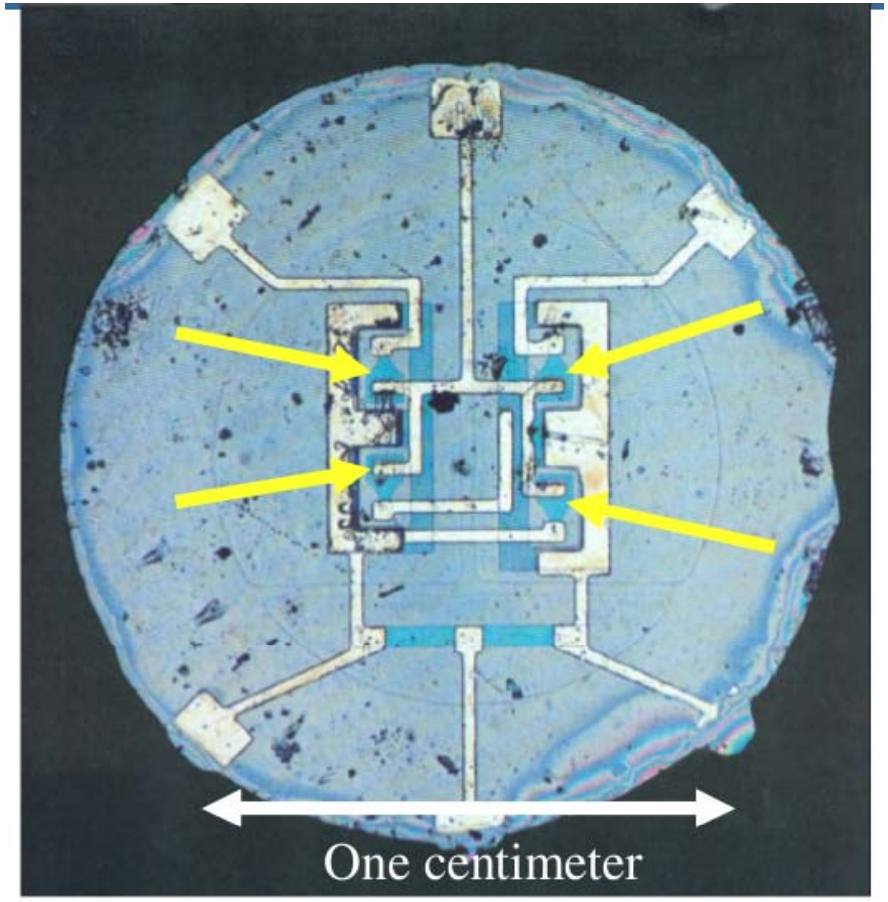


Nobel Prize, 2000

Jack Kilby: Inventor of the first integrated circuit – at Texas Instruments in 1959

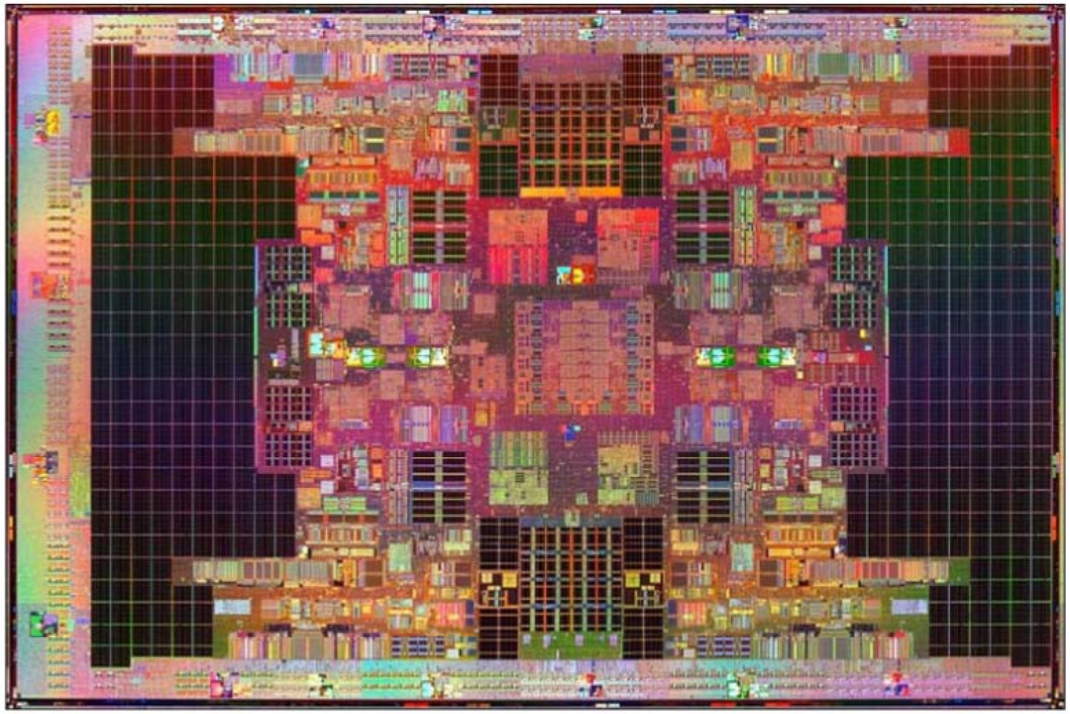


Robret Noyce: First monolitic integrated circuit

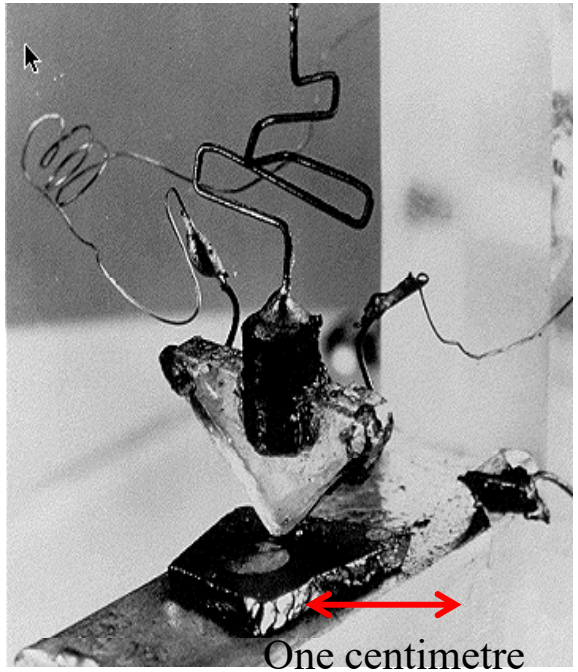


Only 4 transistors!

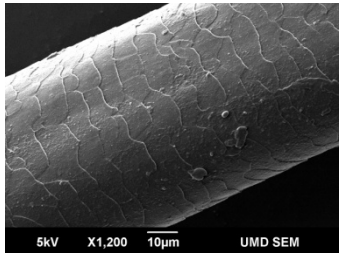
Intel Quad-Core (2,000,000,000 transistors), 2008



One centimeter



The first transistor 1947

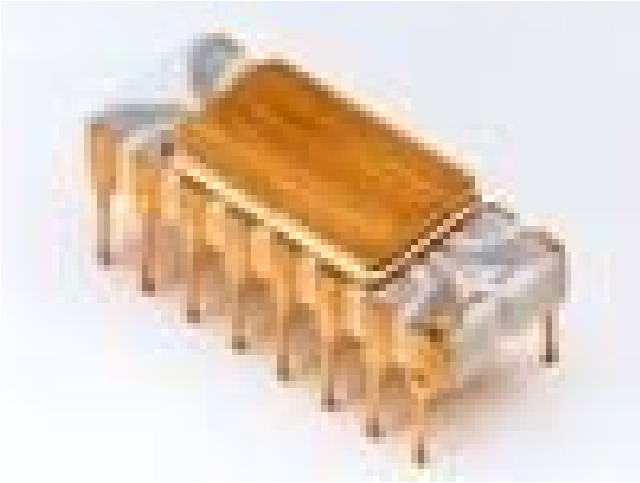


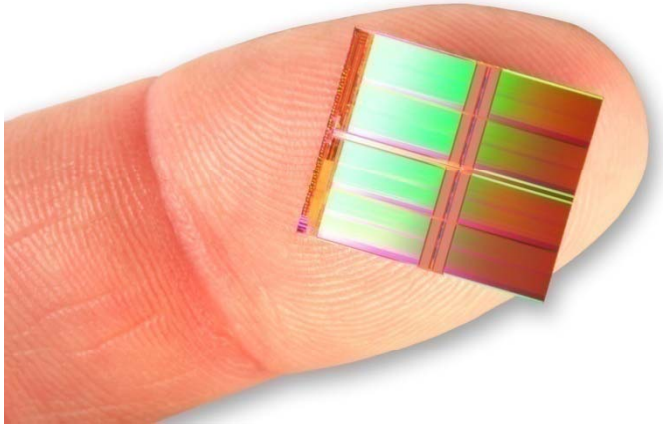
4000 transistors of 22 nm gate length fit across the width of a human hair!

Higher numbers of transistors on a chip ➔

- **High speed of microprocessors**
- **Low cost**
- **Low power consumption**

Past & Present:
Silicon Microprocessors at the 20 nm length scale
(a human hair is about 50,000 nm in diameter)





1971:

Intel 4004. First commercially available microprocessor:

5 kilobits of data (~ a text message)

~600 kHz clock frequency

2011:

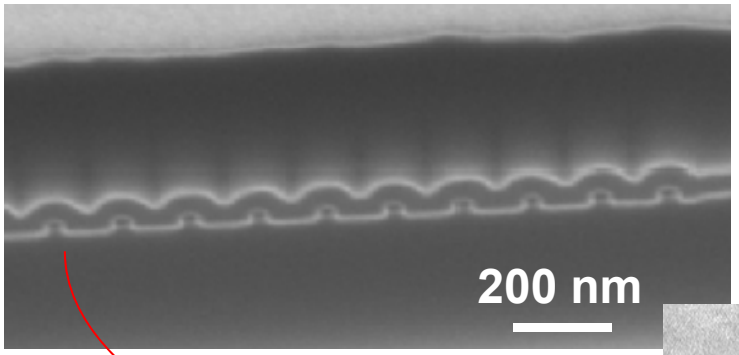
8 x 128 Gbit die

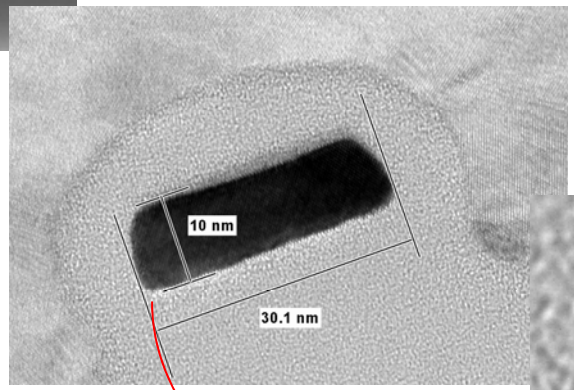
1 Terabit of data (~50,000 photos from a 3 Megapixel camera)

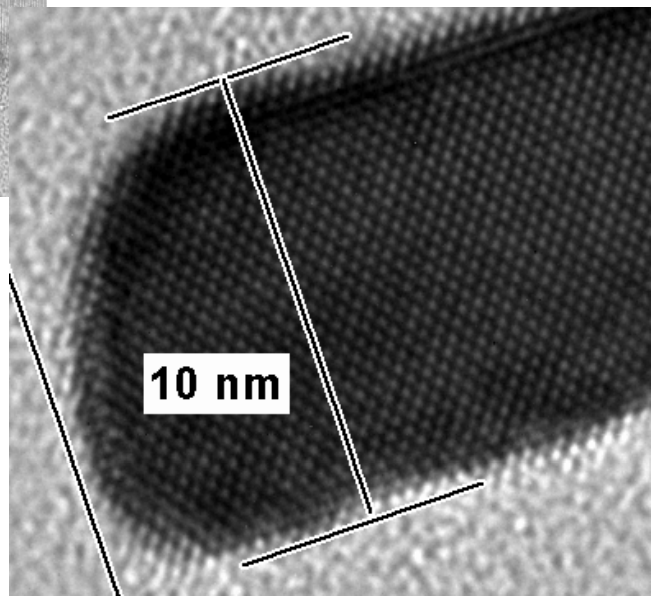
~3 GHz clock frequency

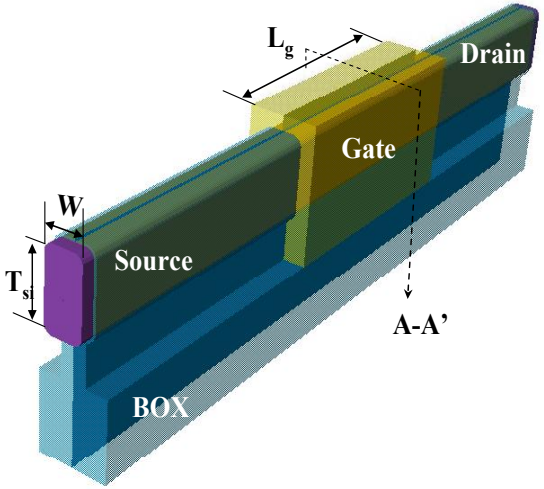
Source: Intel (6/12/11)

Near Future: 3D Nanotransistors



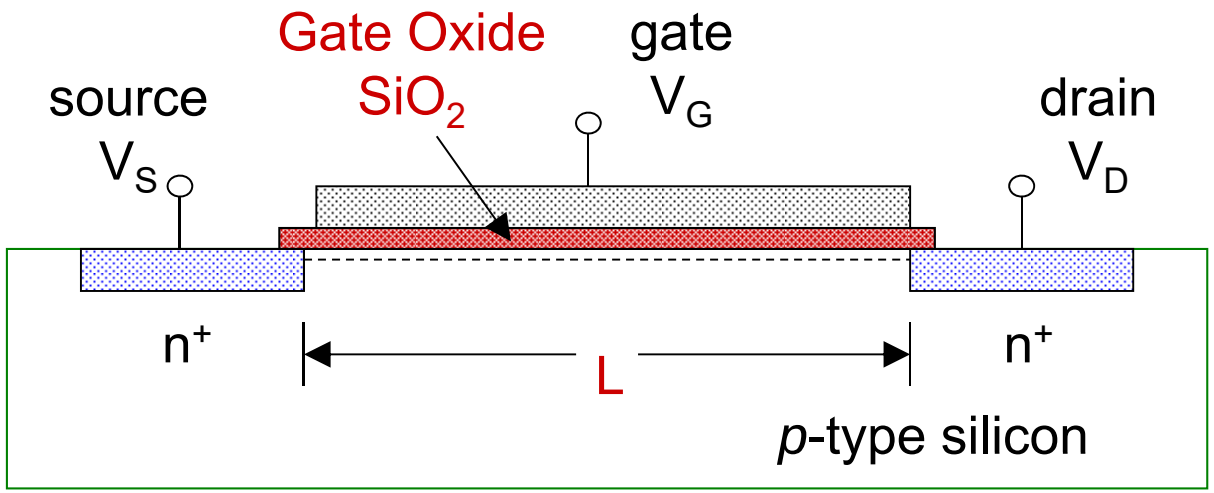






Nanoscale Tri-gate Transistors Fabricated at Tyndall using Electron-Beam Lithography (Prof. J.P. Colinge). Electron microscopy images from Intel Ireland (2014).

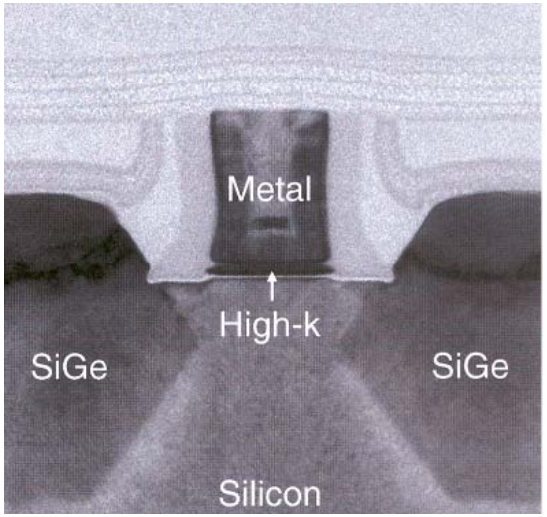
Classical CMOS Field-effect Transistor



- First MOSFET IC's produced in 1963
- SiO_2 was the gate dielectric of choice until 2008
- Channel / gate oxide interface critical to device performance and long-term stability
- L is the channel (gate) length

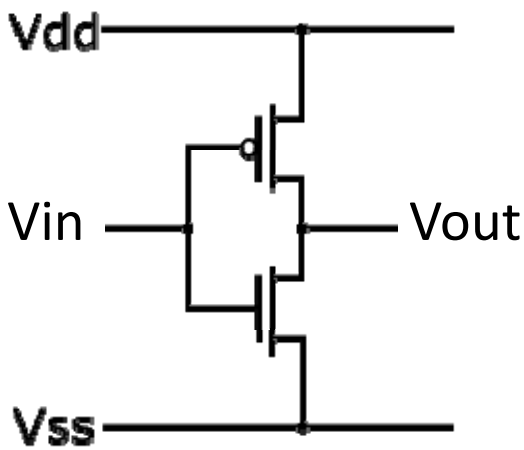
Source: Barry O'Sullivan

MOSFET: Metal Oxide Semiconductor Field Effect Transistor



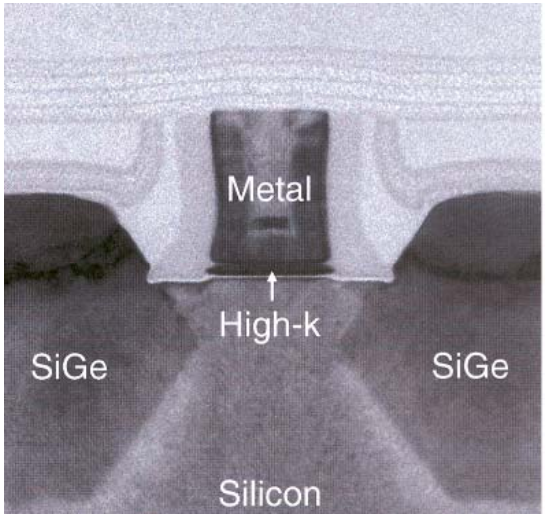
45-nm node
(INTEL)

CMOS Inverter



MOSFETs are Everywhere

MOSFET: Metal Oxide Semiconductor Field Effect Transistor

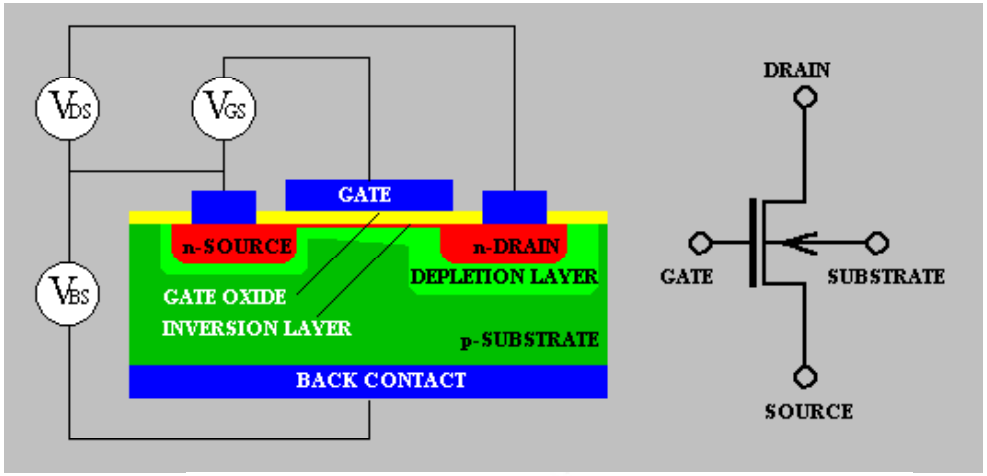


Data centres

Transistor is a switch!

Julius Edgar Lilienfeld , 1925

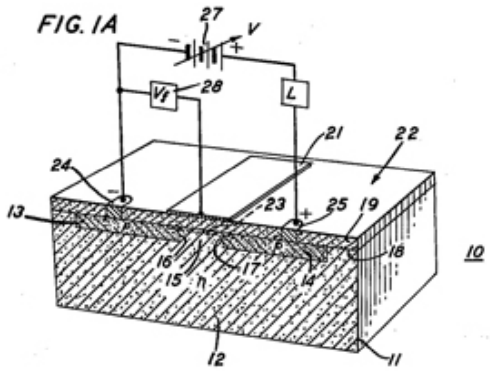
Dawon Kahng, 1959

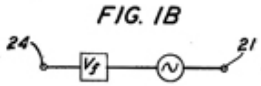


Aug. 27, 1963 DAWON KAHNG 3,102,230

ELECTRIC FIELD CONTROLLED SEMICONDUCTOR DEVICE

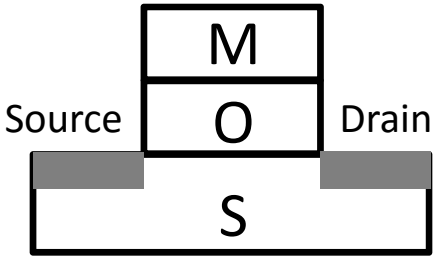
Filed May 31, 1960





MOS Gate Stack

→ Ideal Case



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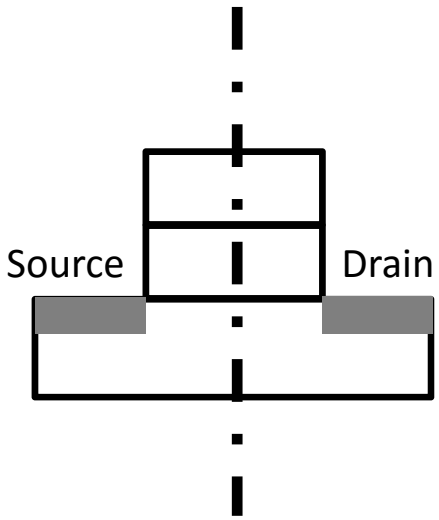
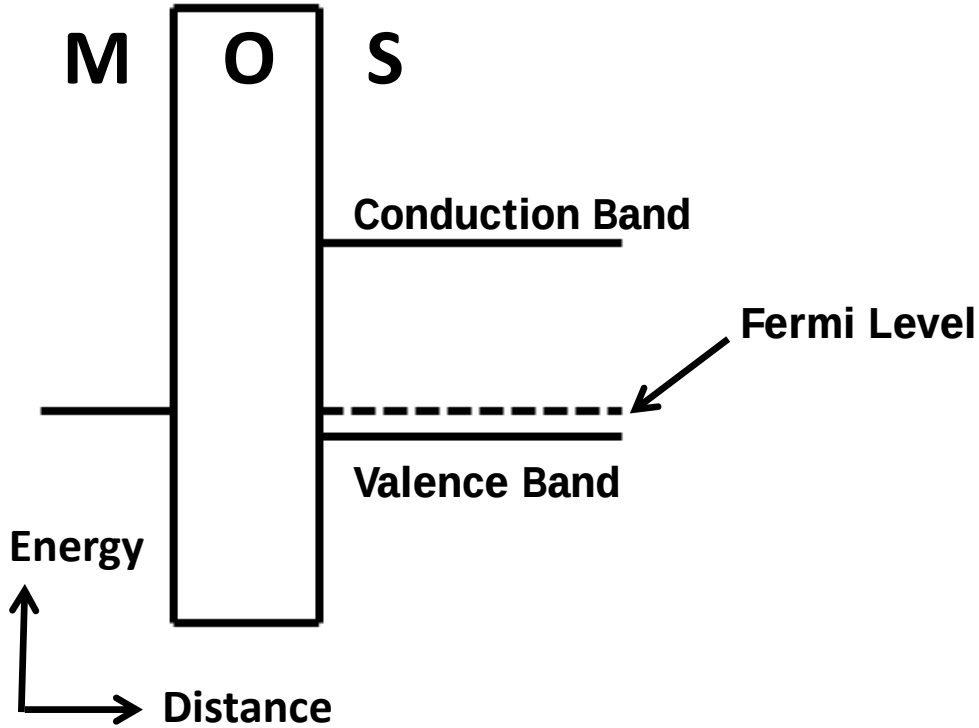
MOS Gate Stack

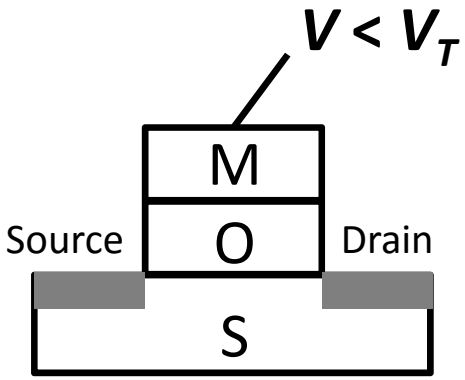
→ Ideal Case



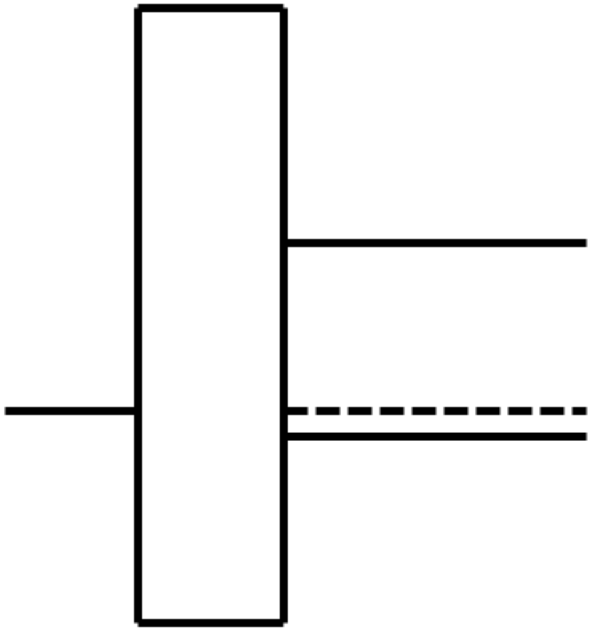


MOS Gate Stack

→ Ideal Case



OFF state



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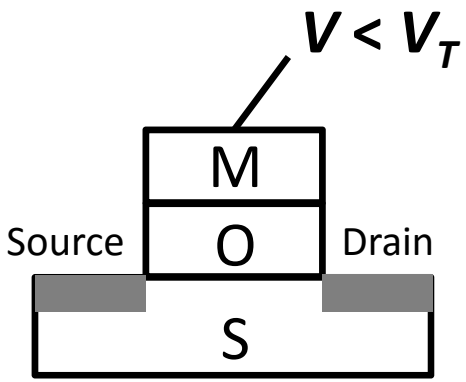
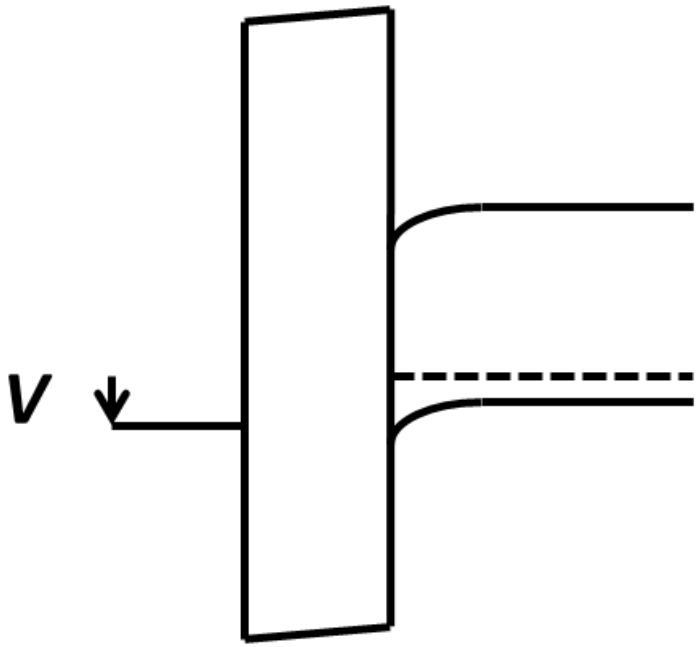
MOS Gate Stack

→ Ideal Case

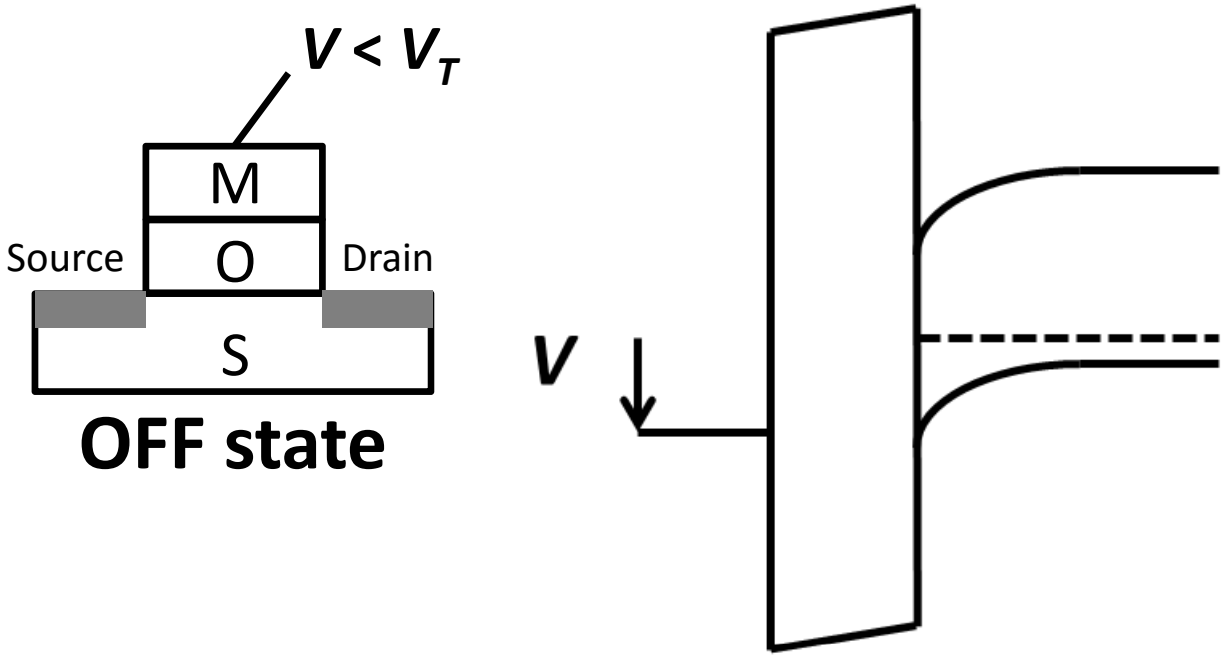


OFF state



MOS Gate Stack

→ Ideal Case

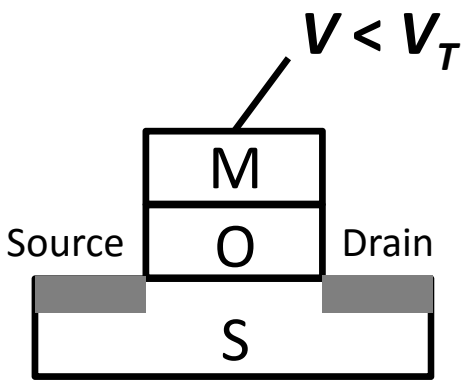


OFF state

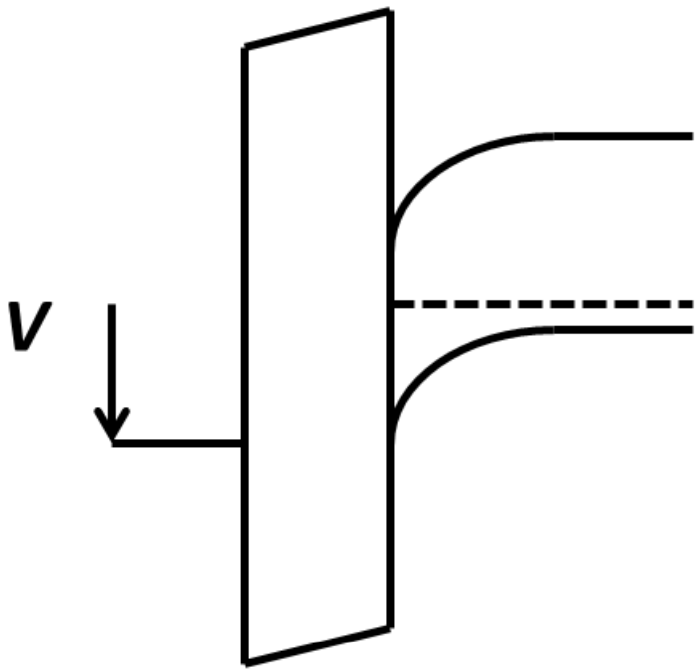
17

MOS Gate Stack

→ Ideal Case

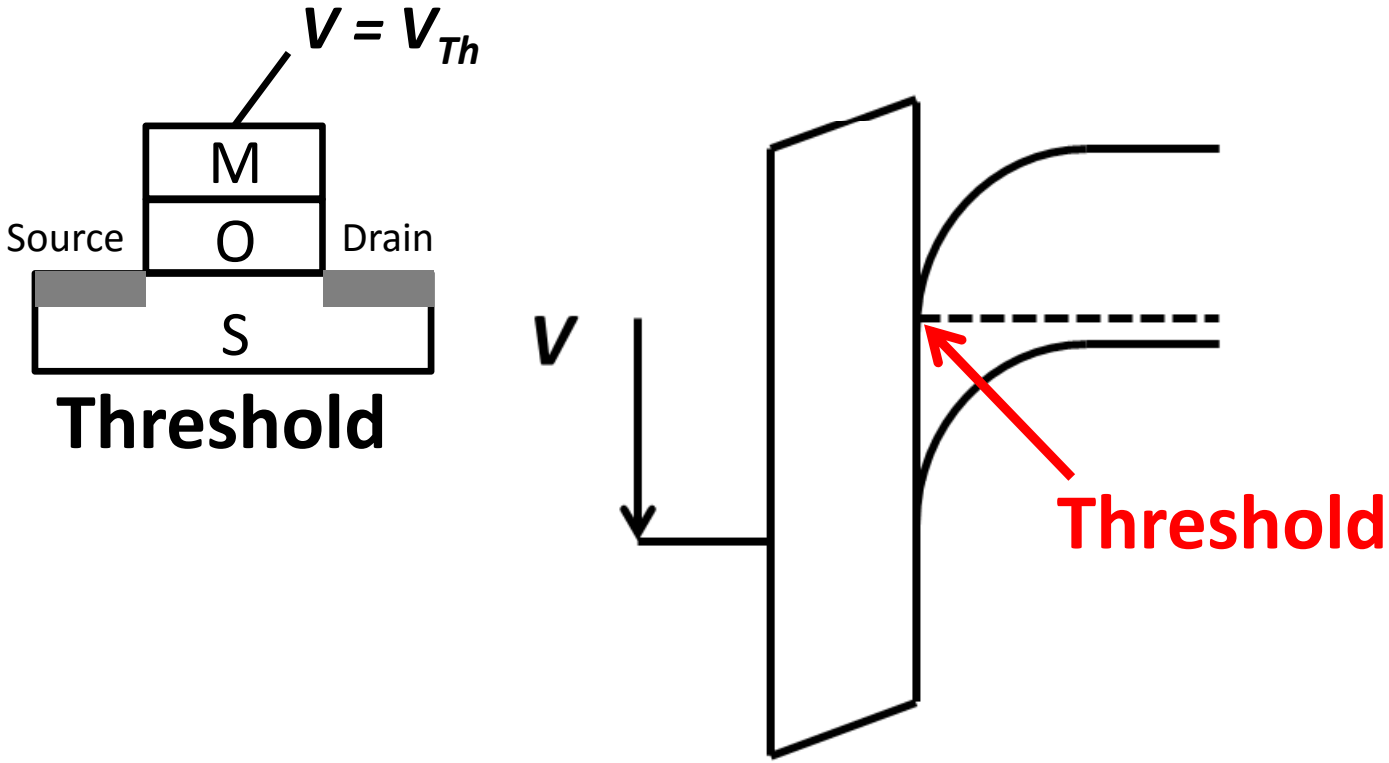


OFF state



MOS Gate Stack

→ Ideal Case



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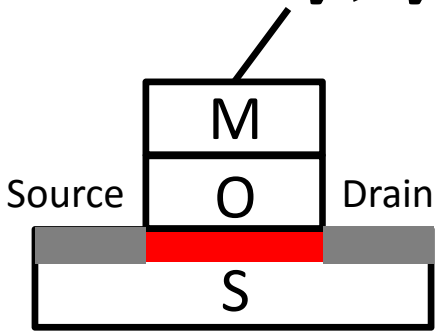
MOS Gate Stack

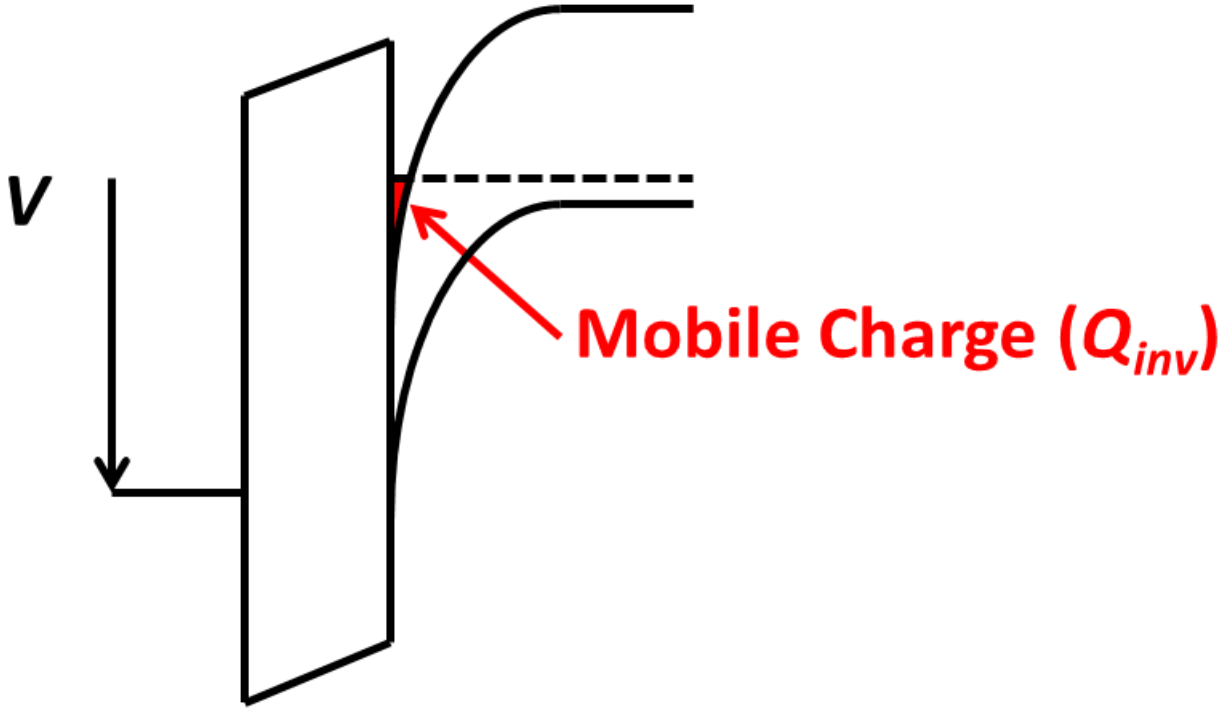
→ Ideal Case

$V > V_{Th}$



ON state

$$Q_{inv} = C_{ox} \cdot (V - V_{Th})$$

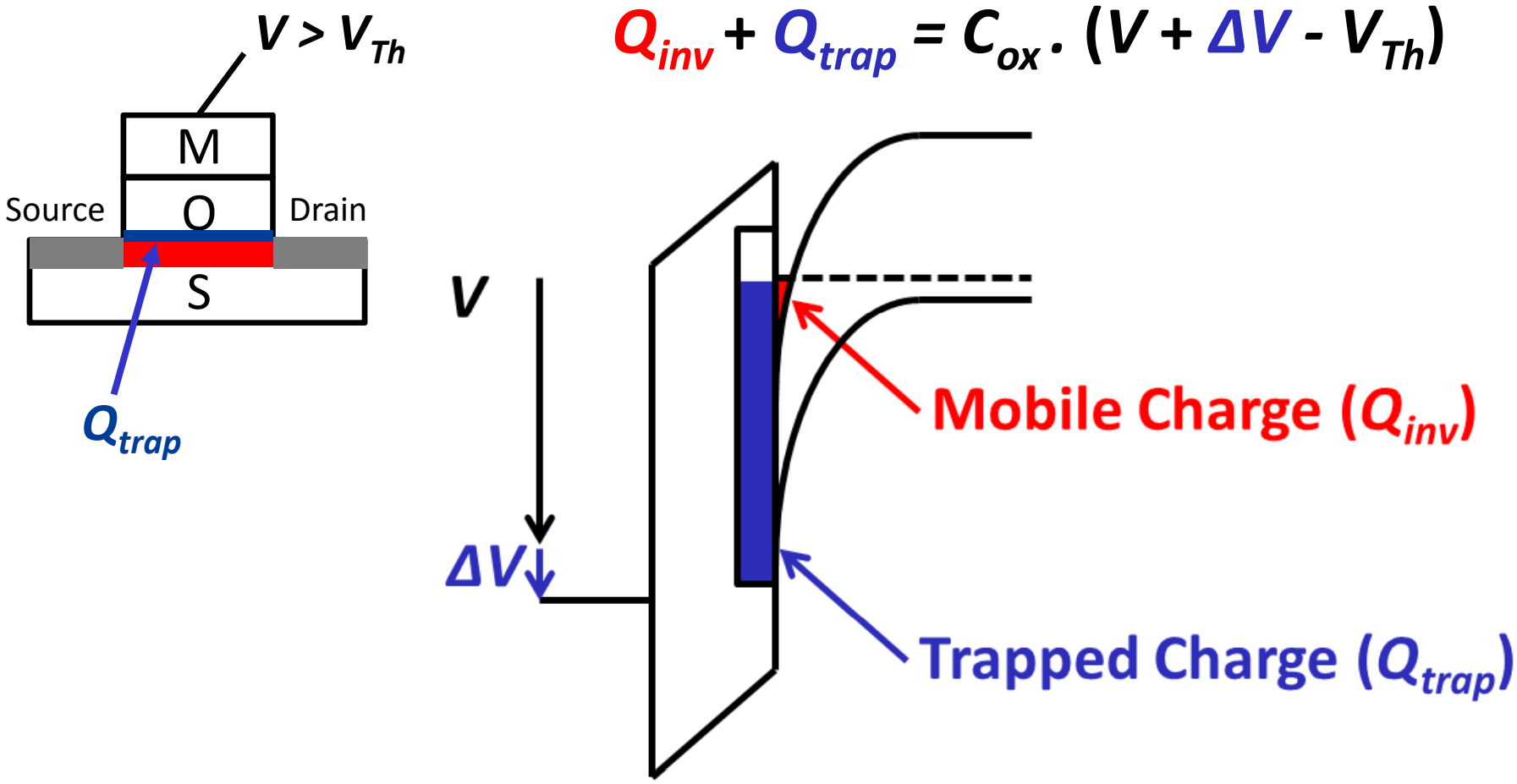


20

MOS Gate Stack

→ Non-ideal Case

$$Q_{inv} + Q_{trap} = C_{ox} \cdot (V + \Delta V - V_{Th})$$



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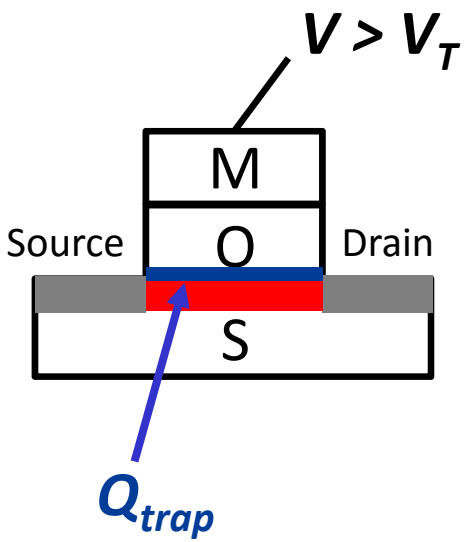
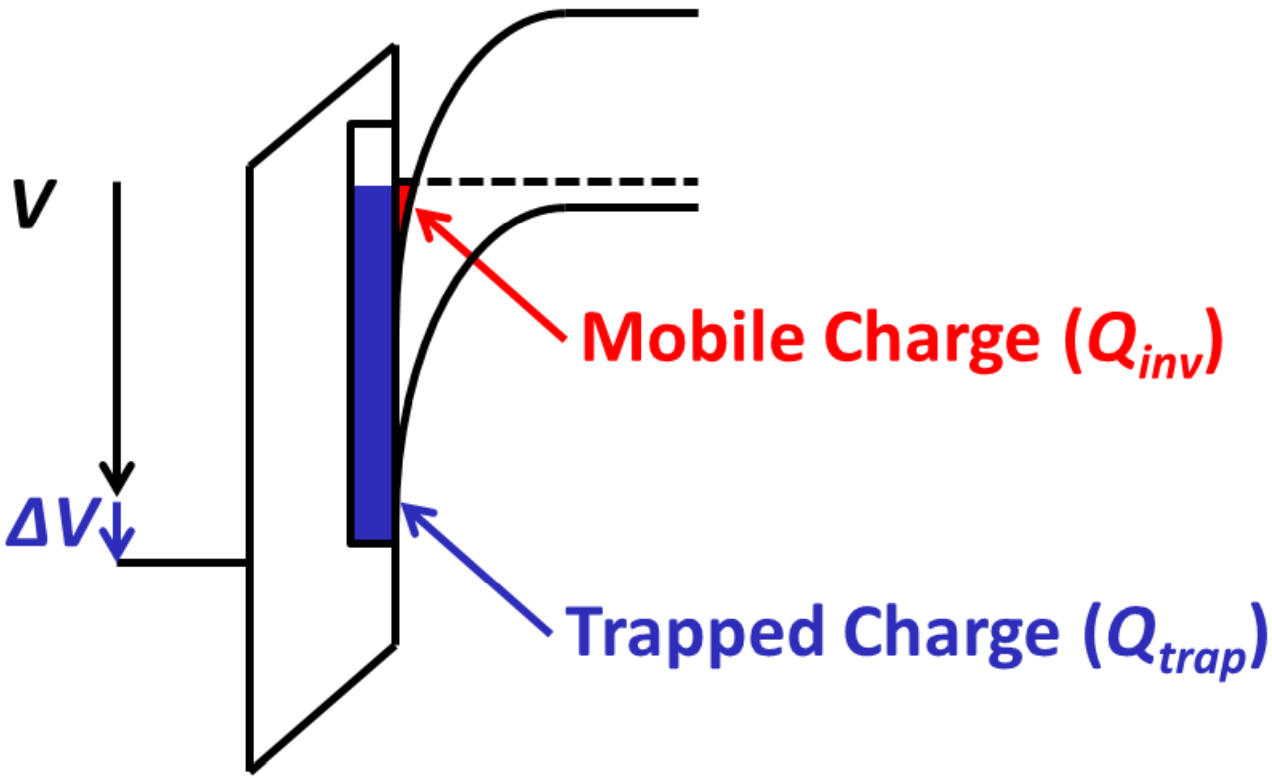
MOS Gate Stack

→ Non-ideal Case

$$Q_{inv} + Q_{trap} = C_{ox} \cdot (V + \Delta V - V_T)$$





ΔV yields degradation of SS

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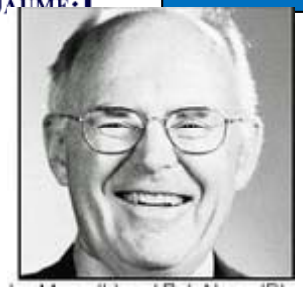
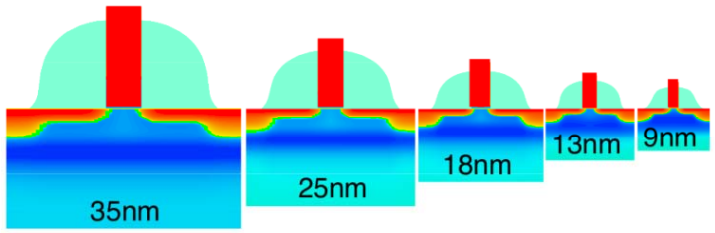
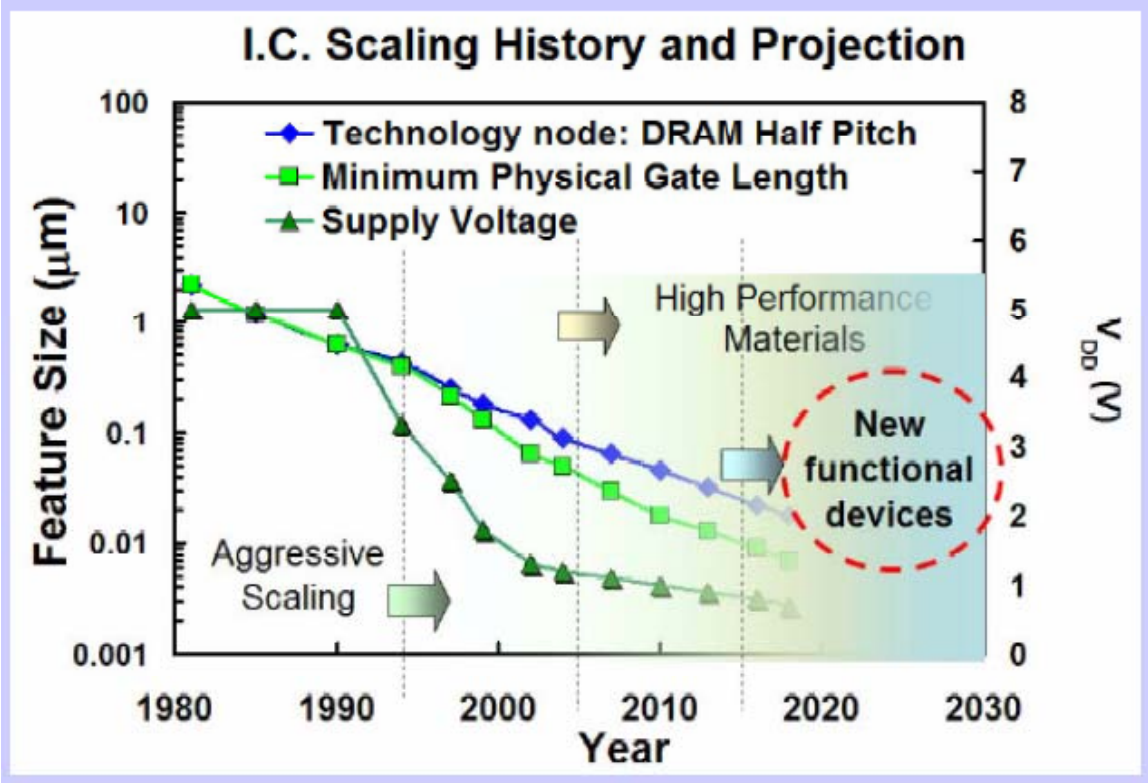
Motivation



Gordon Moore

Number of transistors in ICs had doubled every year from the invention of the IC in 1958 until 1965 and predicted that the trend would continue "for at least ten years"

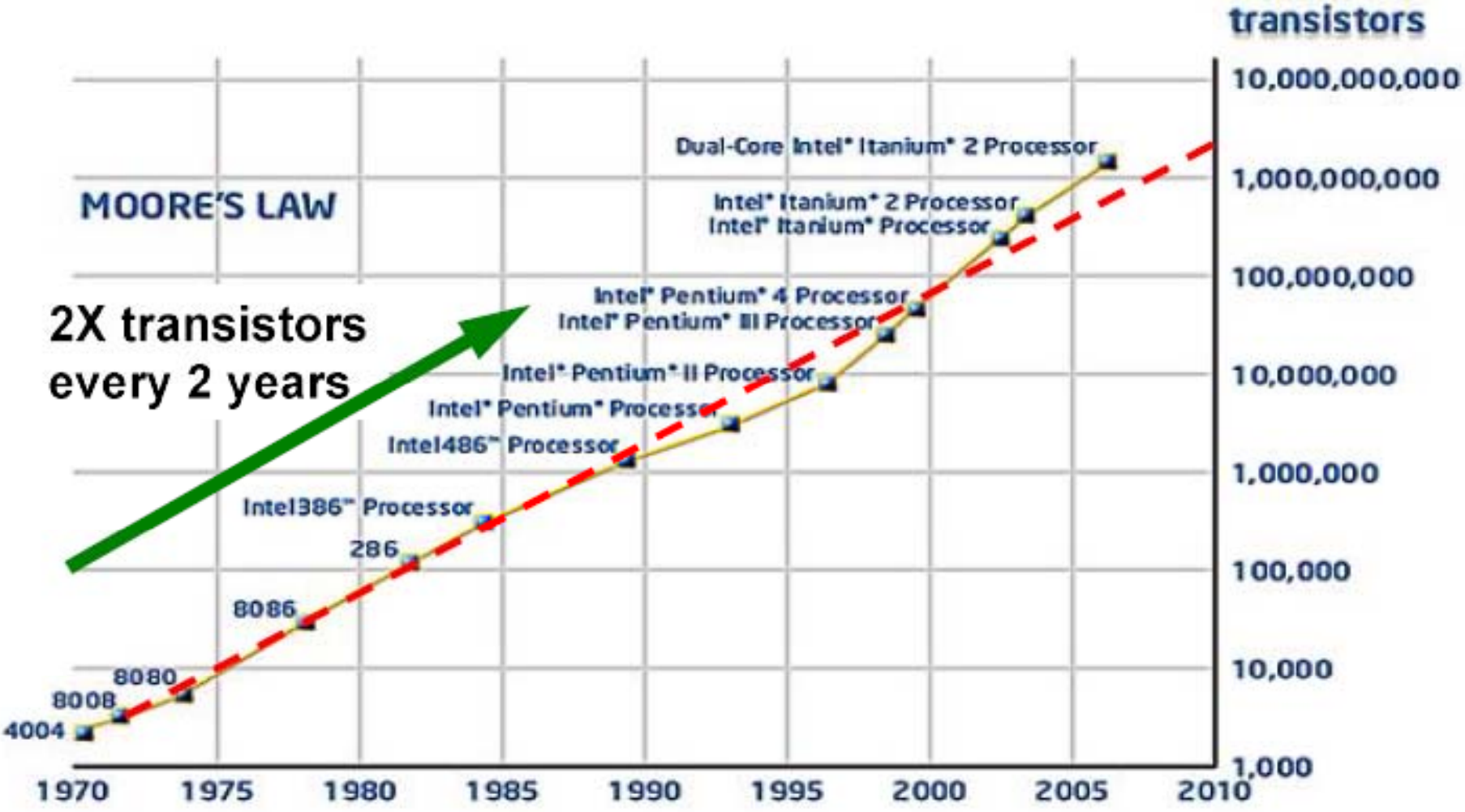




Traditional scaling increasingly challenging ➔ new materials & novel devices

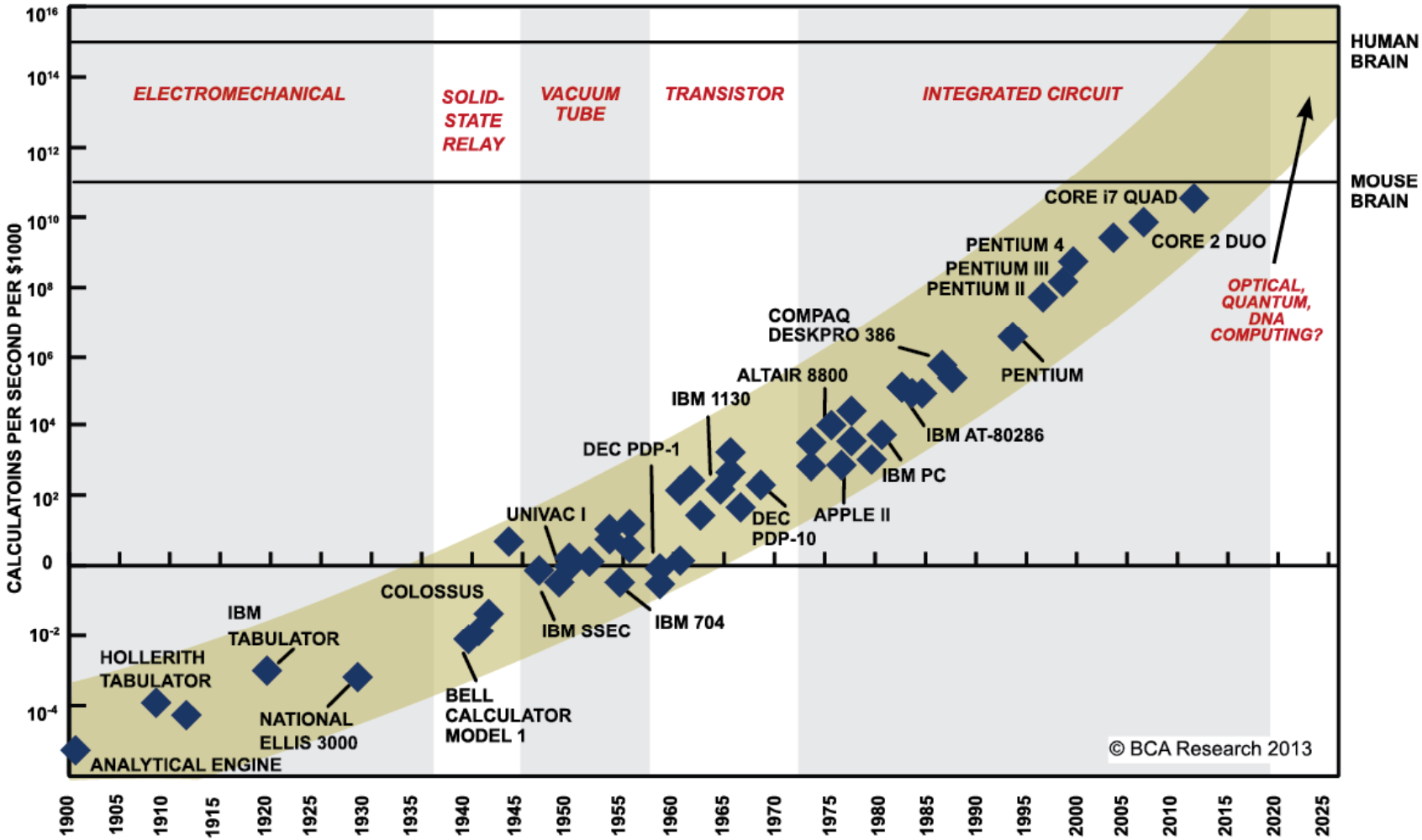
Source ITRS

Moore's Law: Number of transistors per unit area doubles every 2 years



Source: Intel (Oct. 2009)

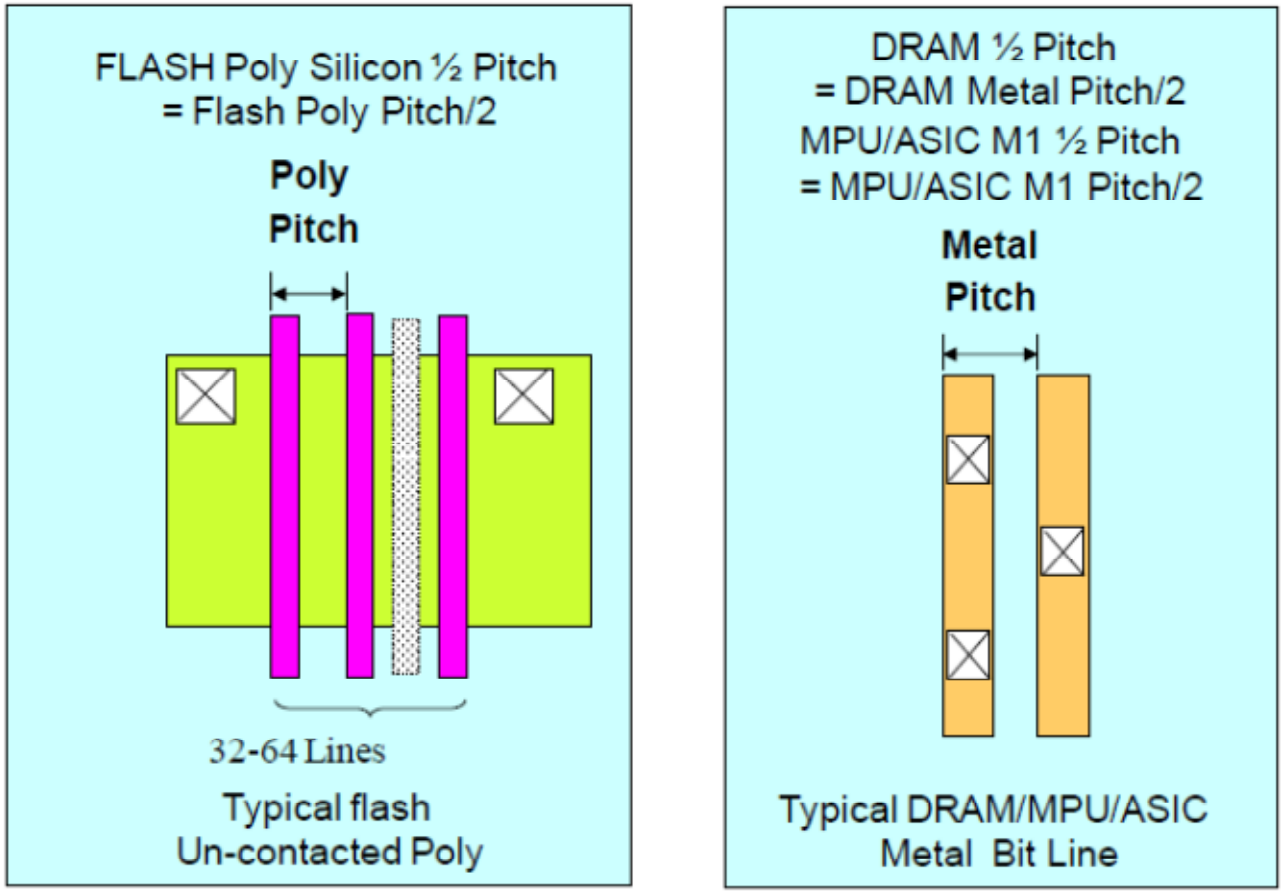
Top-down MOS transistors



SOURCE: RAY KURZWEIL, "THE SINGULARITY IS NEAR: WHEN HUMANS TRANSCEND BIOLOGY", P.67, *THE VIKING PRESS*, 2006. DATAPOINTS BETWEEN 2000 AND 2012 REPRESENT BCA ESTIMATES.

Typical feature size for a given ITRS node/year

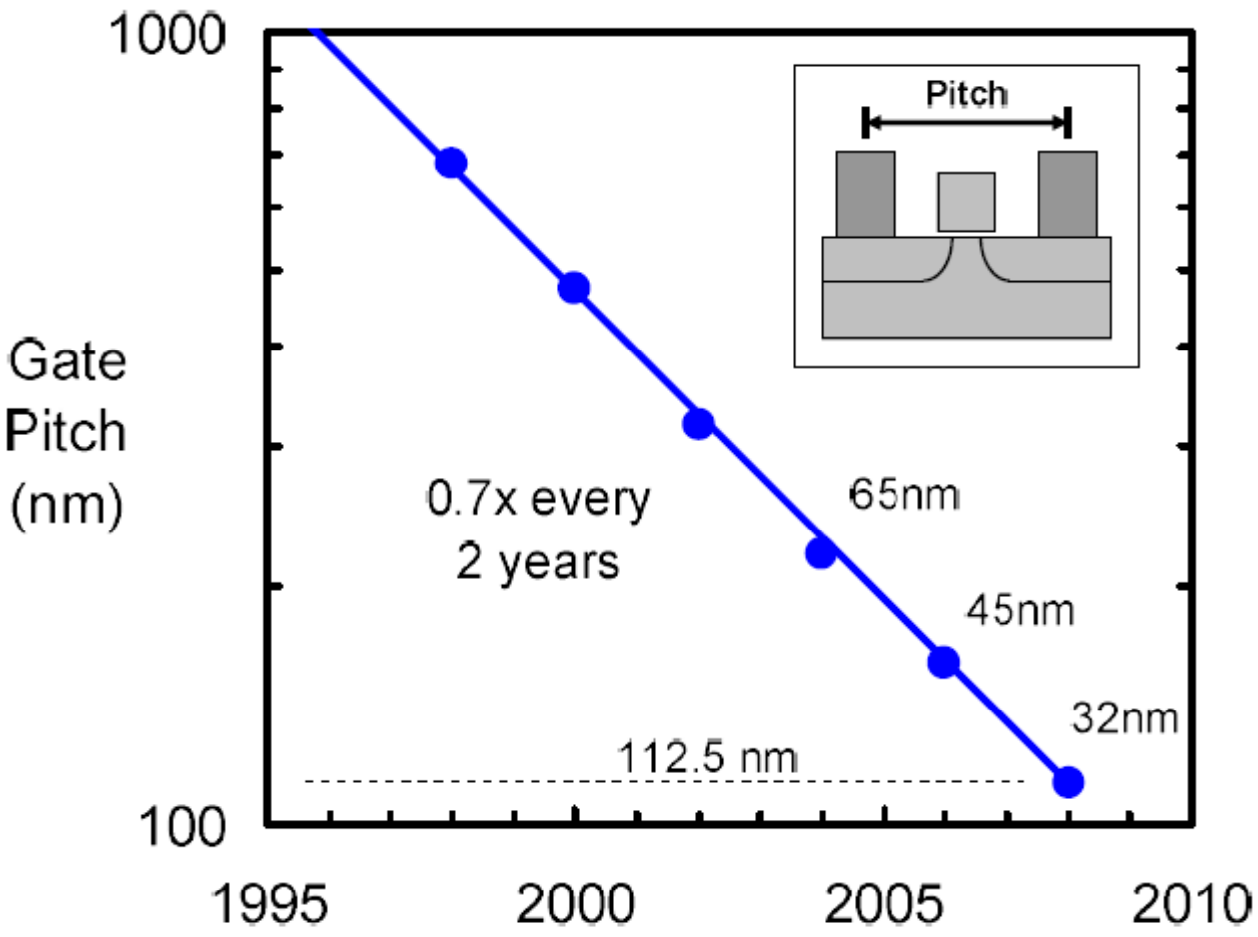
Definitions of **typical** feature size for a given ITRS node/year
NB Some features are even smaller, e.g. gate length



Source ITRS 2011

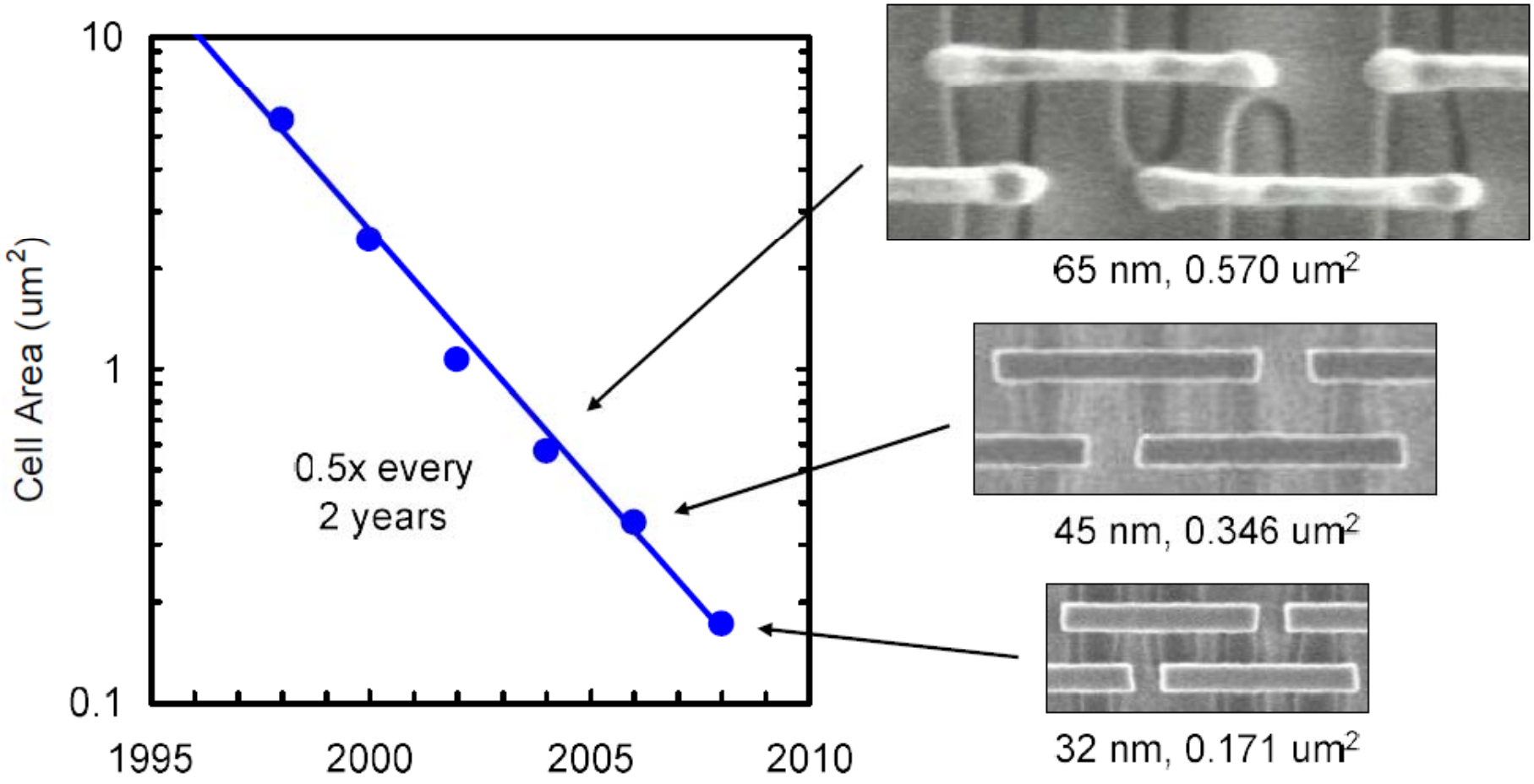
Figure 1 *2011 Definition of Pitches*

Gate Pitch (Intel)



Source: Intel (Oct. 2009)

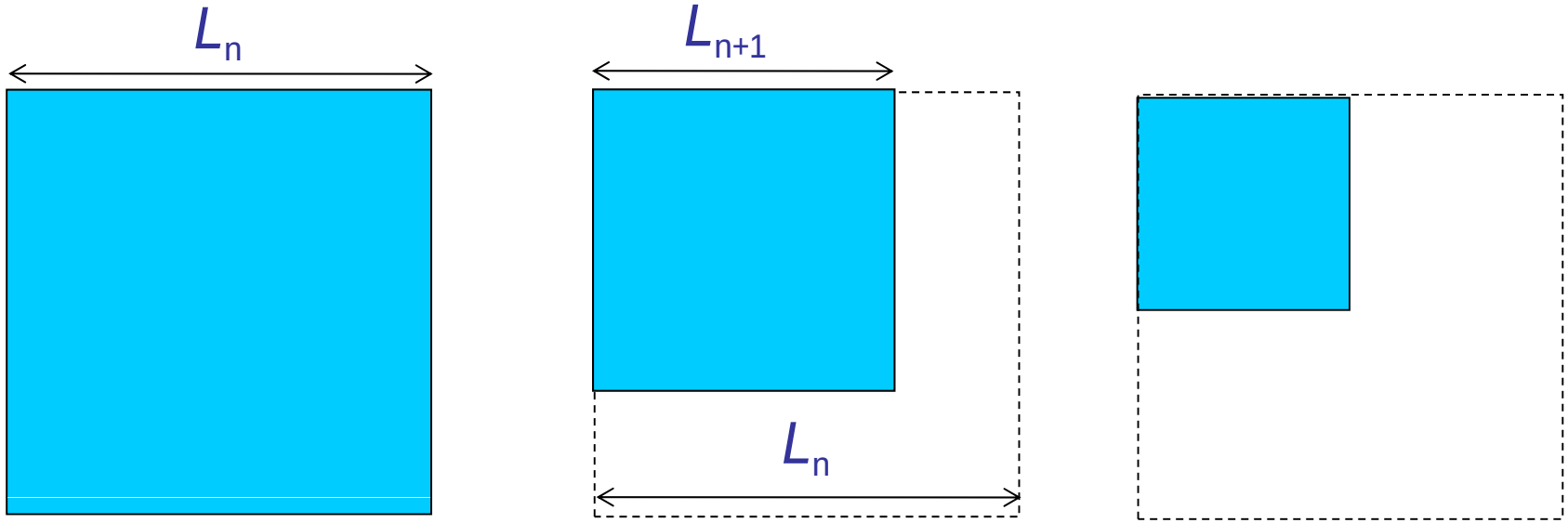
Static Random Access Memory (SRAM) Cell Size



Source: Intel (Oct. 2009)

Scaling Nodes (term gradually being replaced by "Year of First Production" due to differences in scaling rates)

Why: 500 nm, 350 nm, 250 nm, 180 nm, 130 nm, 90 nm, 65 nm, 45 nm, 32 nm ?



Area of 1 transistor:

$A_n = L_n^2$

$A_{n+1} = A_n / 2$

$= L_{n+1}^2$

$\Rightarrow L_{n+1}^2 = L_n^2 / 2$

$\Rightarrow L_{n+1} = L_n / \sqrt{2}$

$A_{n+2} = A_{n+1} / 2$

$= A_n / 4$

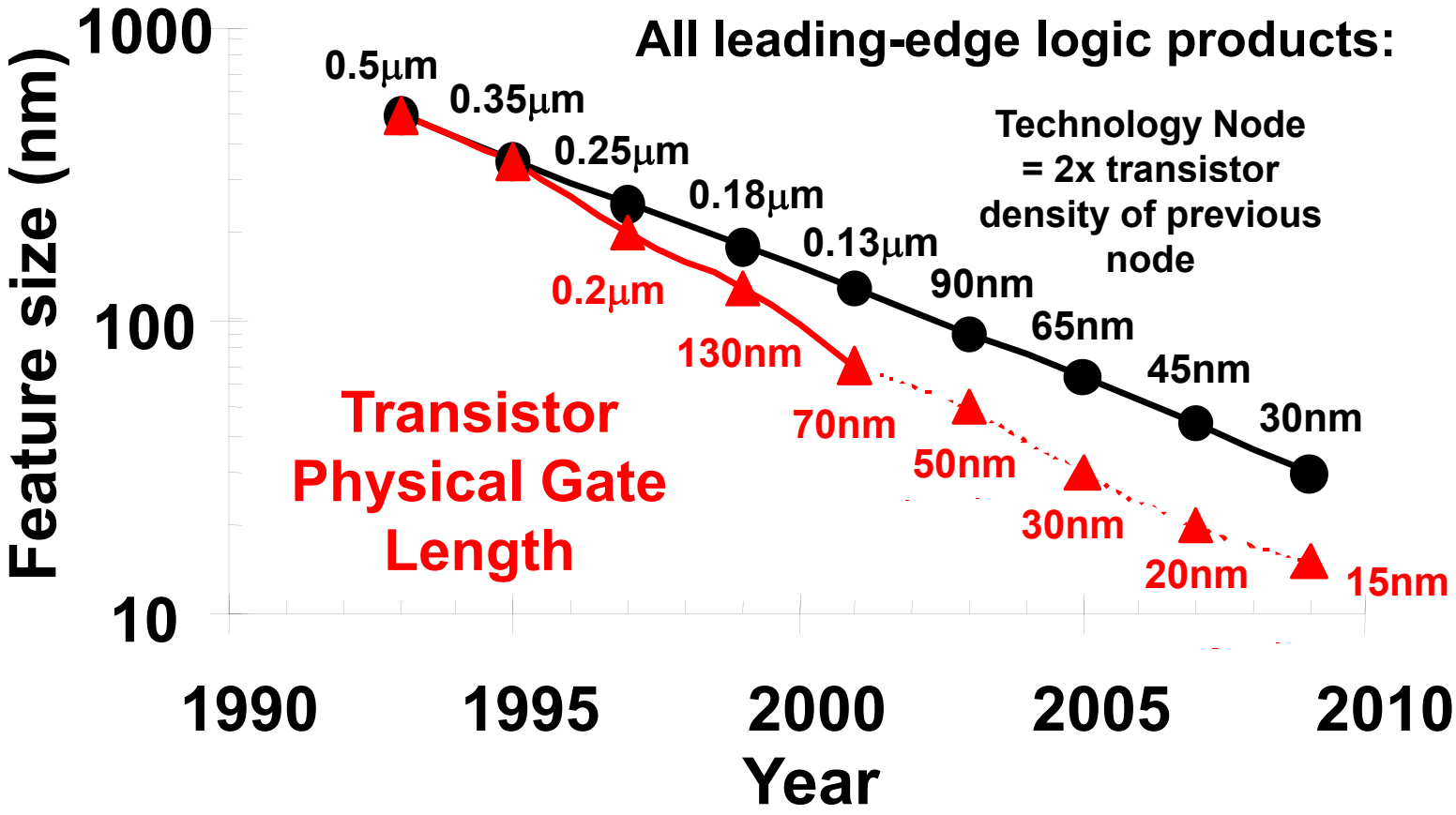
$= L_{n+2}^2$

$\Rightarrow L_{n+2}^2 = L_n^2 / 4$

$\Rightarrow L_{n+2} = L_n / 2$

$\sqrt{2} \approx 1.4 \qquad 1/\sqrt{2} \approx 0.7$

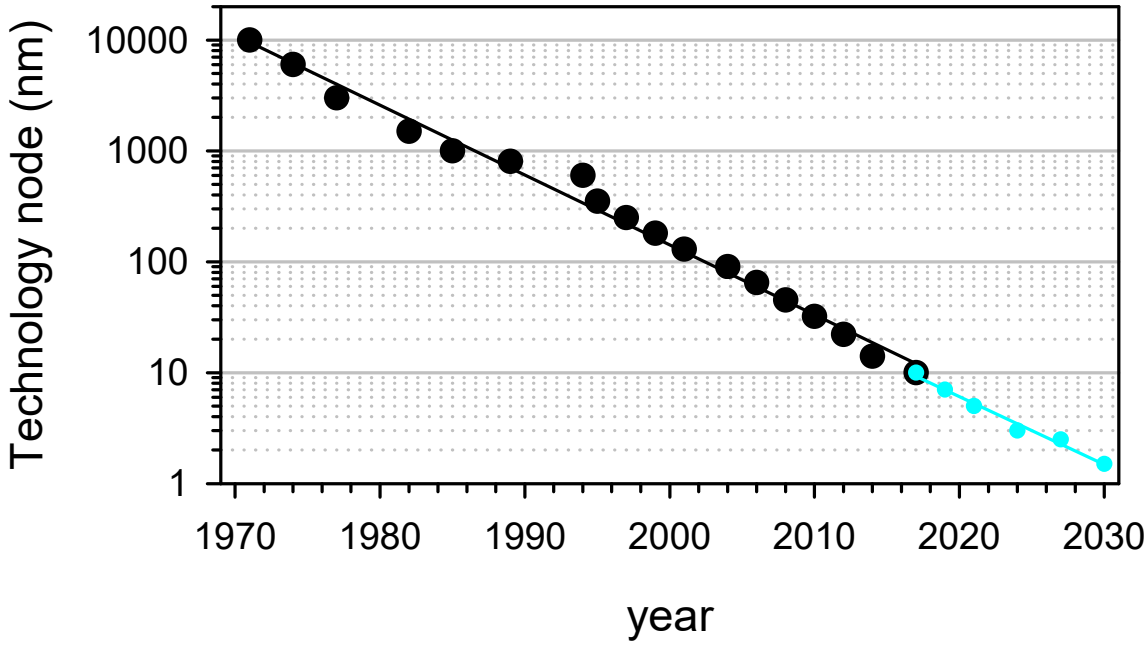
Moore's Law driven by scaling



Source ITRS 2001

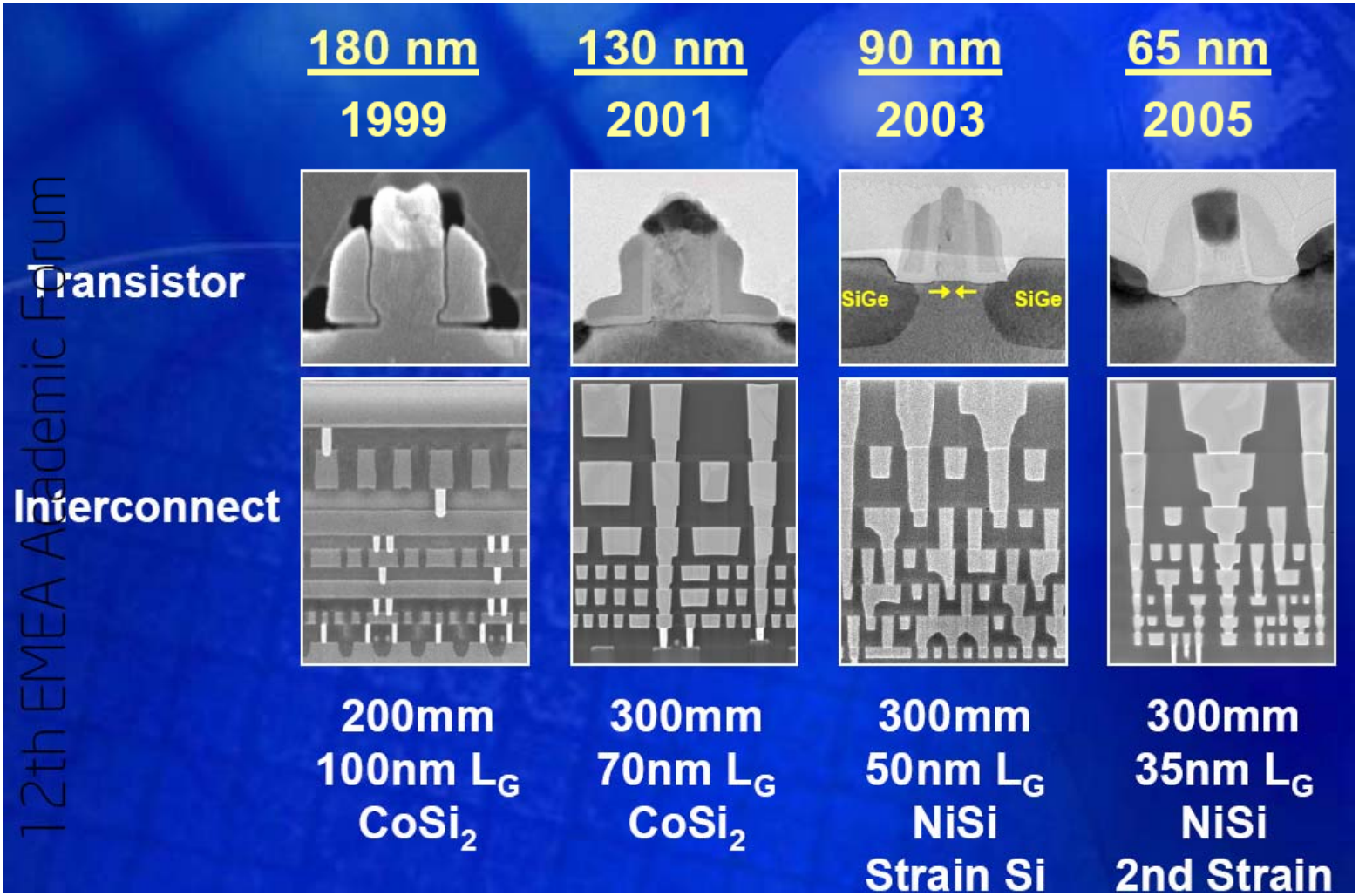
Moore's Law driven by scaling

All leading-edge logic products:



Source: ITRS 2015

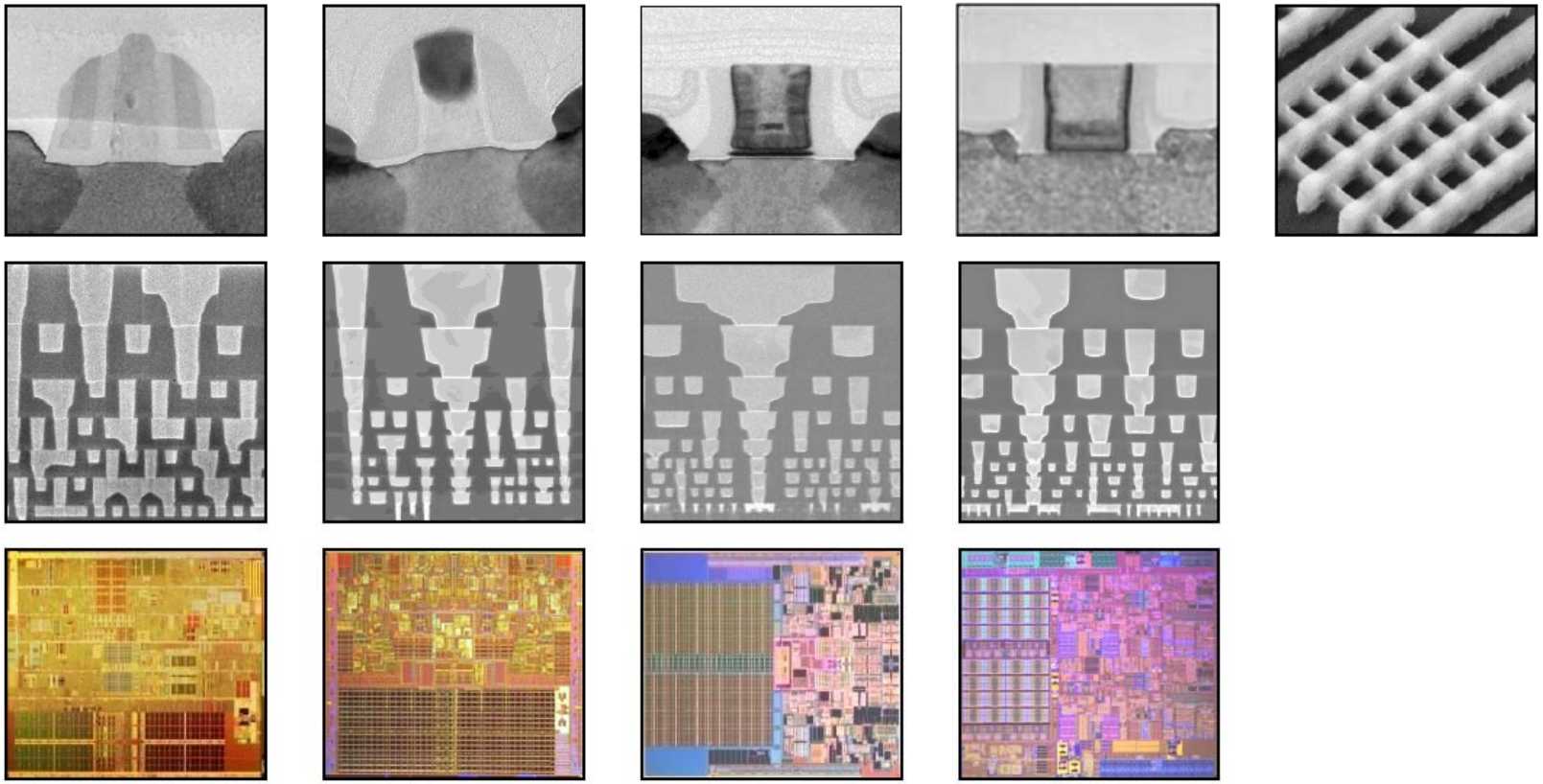
Top-down MOS transistors



J. Maiz, Intel, 2007

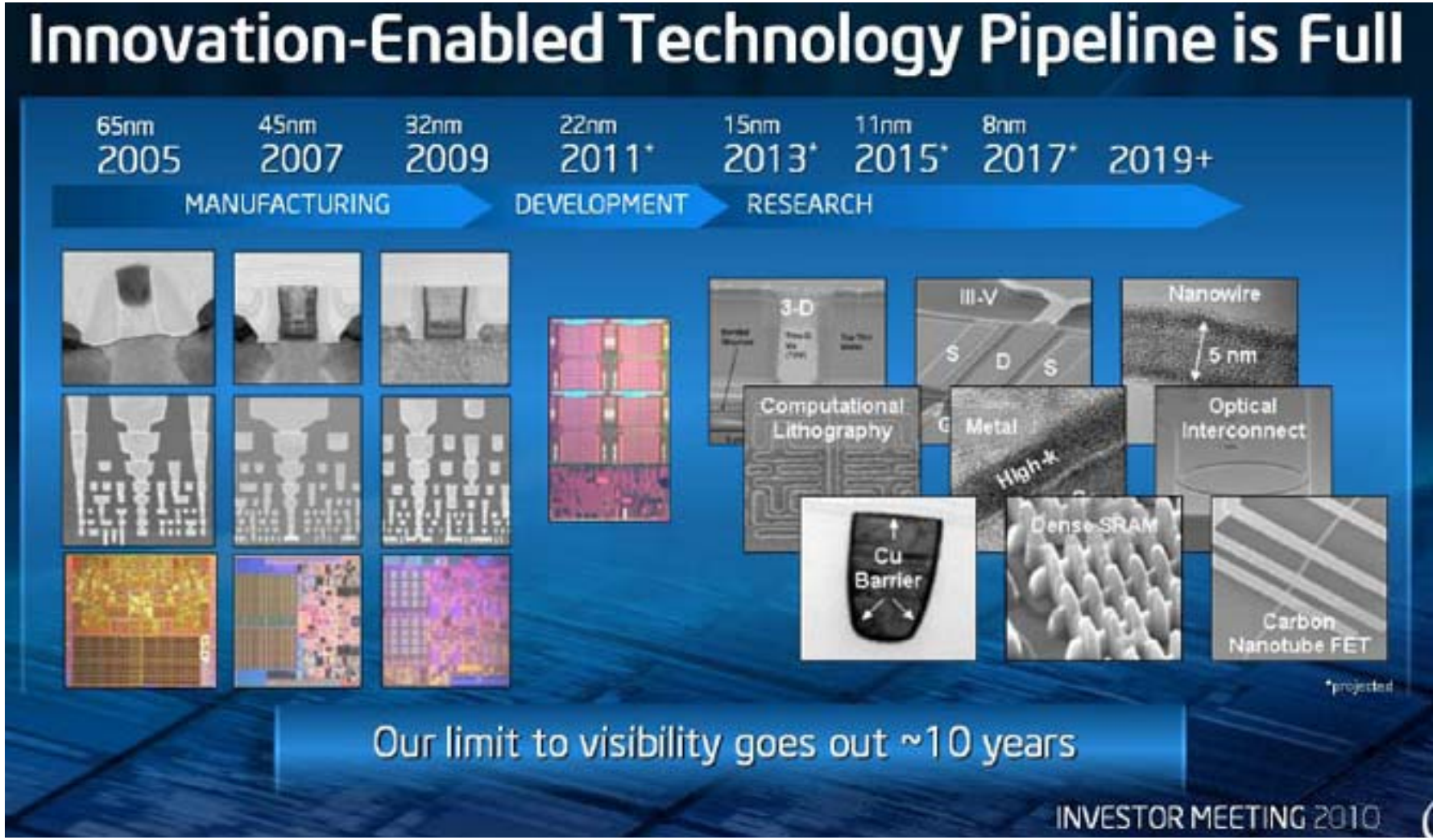
Top-down MOS transistors

90 nm	65 nm	45 nm	32 nm	22 nm	14 nm
2003	2005	2007	2009	2011	2014



Intel, 2011

Top-down MOS transistors



Intel, 2010

Predicted Feature Sizes in CMOS

Table B *ITRS Table Structure—Key Lithography-related Characteristics by Product*

Near-term Years

Year of Production	2011	2012	2013	2014	2015	2016	2017	2018
Flash ½ Pitch (nm) (un-contacted Poly)(f)[2]	22	20	18	17	15	14.2	13.0	11.9
DRAM ½ Pitch (nm) (contacted)[1,2]	36	32	28	25	23	20.0	17.9	15.9
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)[1,2]	38	32	27	24	21	18.9	16.9	15.0
MPU High-Performance Printed Gate Length (GLpr) (nm) ††[1]	35	31	28	25	22	19.8	17.7	15.7
MPU High-Performance Physical Gate Length (GLph) (nm)[1]	24	22	20	18	17	15.3	14.0	12.8
ASIC/Low Operating Power Printed Gate Length (nm) ††[1]	41	35	31	25	22	19.8	17.7	15.7
ASIC/Low Operating Power Physical Gate Length (nm)[1]	26	24	21	19.4	17.6	16.0	14.5	13.1
ASIC/Low Standby Power Physical Gate Length (nm)[1]	30	27	24	22	20	17.5	15.7	14.1
MPU High-Performance Etch Ratio GLpr/GLph [1]	1.4589	1.4239	1.3898	1.3564	1.3239	1.2921	1.2611	1.2309
MPU Low Operating Power Etch Ratio GLpr/GLph [1]	1.5599	1.4972	1.4706	1.2869	1.2640	1.2416	1.2196	1.1979

NB: Sizes are predicted,
manufacturing solutions have not been identified/optimised for all nodes.

Source ITRS '11, Executive Summary

Predicted Feature Sizes in CMOS

Near-term Years

Year of Production	2011	2012	2013	2014	2015	2016
Flash ½ Pitch (nm) (un-contacted Poly)(f)[2]	22	20	18	17	15	14.2
DRAM ½ Pitch (nm) (contacted)[1,2]	36	32	28	25	23	20.0
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)[1,2]	38	32	27	24	21	18.9
MPU High-Performance Printed Gate Length (GLpr) (nm) ††[1]	35	31	28	25	22	19.8
MPU High-Performance Physical Gate Length (GLph) (nm)[1]	24	22	20	18	17	15.3

Long-term Years

Year of Production	2019	2020	2021	2022	2023	2024	2025	2026
Flash ½ Pitch (nm) (un-contacted Poly)(f)[2]	10.9	10.0	8.9	8.0	8.0	8.0	8.0	8.0
DRAM ½ Pitch (nm) (contacted)[1,2]	14.2	12.6	11.3	10.0	8.9	8.0	7.1	6.3
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)[1,2]	13.4	11.9	10.6	9.5	8.4	7.5	6.7	6.0
MPU High-Performance Printed Gate Length (GLpr) (nm) ††[1]	14.0	12.5	11.1	9.9	8.8	7.9	6.79	5.87
MPU High-Performance Physical Gate Length (GLph) (nm)[1]	11.7	10.6	9.7	8.9	8.1	7.4	6.6	5.9

NB: Sizes are predicted,
manufacturing solutions have not been identified/optimised for all nodes.

Source ITRS '11, Executive Summary

Lithography Challenges (Near Term)

Year of Production	2011	2012	2013	2014	2015	2016	2017	2018
DRAM ½ pitch (nm) (contacted)	36	32	28	25	23	20.0	17.9	15.9
DRAM								
DRAM ½ pitch (nm)	36	32	28	25	23	20	18	16
CD control (3 sigma) (nm) [B]	3.7	3.3	2.9	2.6	2.3	2.1	1.9	1.7
Contact in resist (nm) - Note Optical now, EUV later	55	55	55	55	29	26	23	21
Contact after etch (nm)	36	32	28	25	23	20	18	16
Overlay [A] (3 sigma) (nm)	7.1	6.4	5.7	5.1	4.5	4.0	3.6	3.2
k1 (13.5nm) EUVL	0.66	0.59	0.52	0.47	0.55	0.49	0.44	0.51
Flash								
Flash ½ pitch (nm) (un-contacted poly)	22	20	18	17	15	14.2	13.0	11.9
CD control (3 sigma) (nm) [B]	2.3	2.1	1.9	1.8	1.6	1.5	1.4	1.2
Bit line Contact Pitch (nm) [D]	131	120	110	101	93	113	104	95
Contact after etch (nm)	36	32	28	25	23	20	18	16
Overlay [A] (3 sigma) (nm)	7.2	6.6	6.1	5.6	5.1	4.7	4.3	3.9
k1 (13.5nm) EUVL	0.42	0.39	0.35	0.32	0.38	0.35	0.32	0.38
MPU / Logic								
MPU/ASIC Metal 1 (M1) ½ pitch (nm)	38	32	27	24	21	18.9	16.9	15.0
MPU gate in resist (nm)	35	31	28	25	22	20	18	16
MPU physical gate length (nm) *	24	22	20	18	17	15	14	13
Gate CD control (3 sigma) (nm) [B] **	2.5	2.3	2.1	1.9	1.7	1.6	1.5	1.3
Contact in resist (nm)	55	55	55	55	28	25	22	20
Contact after etch (nm)	43	36	30	27	24	21	19	17
Overlay [A] (3 sigma) (nm)	7.6	6.4	5.4	4.8	4.2	3.8	3.4	3.0
k1 (13.5nm) EUVL	0.70	0.59	0.50	0.44	0.52	0.46	0.41	0.48

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known

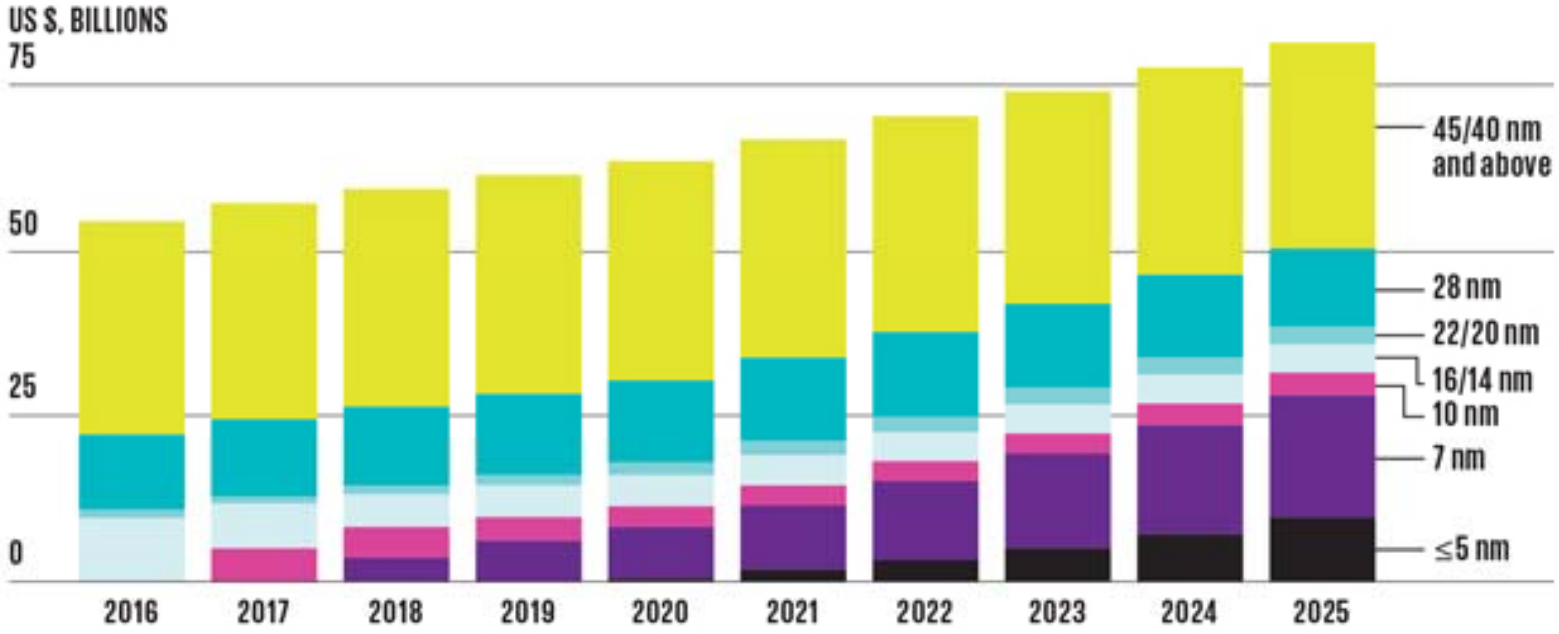
Source: ITRS '11, Lithography Section
http://www.itrs2.net/itrs-reports.html

Lithography Challenges (Near Term)

YEAR OF PRODUCTION	2015	2017	2019	2021	2024	2027	2030
Logic device technology naming	P70M56	P48M36	P42M24	P32M20	P24M12G1	P24M12G2	P24M12G3
Logic industry "Node Range" Labeling (nm)	"16/14"	"11/10"	"8/7"	"6/5"	"4/3"	"3/2.5"	"2/1.5"
Logic device structure options	finFET FDSOI	finFET FDSOI	finFET LGAA	finFET LGAA VGAA	VGAA, M3D	VGAA, M3D	VGAA, M3D
DRAM							
DRAM minimum ½ pitch (nm)	24	22	18.0	15.0	12.0	9.2	7.7
CD control (3 sigma) (nm) [B]	2.4	2.2	1.8	1.5	1.2	0.9	0.8
Mininum contact/via after etch (nm) [H]	24	22	18	15	12.0	9.2	7.7
Minimum contact/via pitch(nm)[H]	72	66	54	45	36	28	23
Overlay (3 sigma) (nm) [A]	4.8	4.4	3.6	3.0	2.4	1.8	1.5
Flash							
2D Flash ½ pitch (nm) (un-contacted poly)	15	14	12	12	12	12	12
Flash 3D Layer half-pitch targets (nm)	80.0	80.0	80.0	80.0	80.0	80.0	80.0
3D NAND minimum metal pitch(nm)	20.0	20.0	20.0	20.0	20.0	20.0	20.0
CD control (3 sigma) (nm) [B]	1.5	1.4	1.2	1.2	1.2	1.2	1.2
Overlay (3 sigma) (nm) [A]	5.1	4.7	3.9	3.9	3.9	3.9	3.9
MPU / Logic							
MPU/ASIC Minimum Metal ½ pitch (nm)	26	18	12	10	6.0	6.0	6.0
MPU/ASIC finFET fin minimum 1/2 pitch (nm)	21	18	12				
Lateral Gate All Around (LGAA) 1/2 pitch			12	10			
Vertical Gate All Around (VGAA) 1/2 pitch				10	6.0	6.0	6.0
Contacted poly half pitch (nm)	35	24	21	16			
Physical Gate Length for HP Logic (nm)	24	18	14	10			
Vertical Gate All Around (VGAA) pitch (nm)				20	12	12	12
Gate CD control (3 sigma) (nm) [B]	2.4	1.8	1.4	1.0	-	-	-
Metal CD control (3 sigma) (nm) [B]	2.6	1.8	1.2	1.0	0.6	0.6	0.6
Fin CD control (3 sigma) (nm) [B]	0.40	0.30	0.30				
FIN or LGAA LER [C]	0.40	0.30	0.30				
Gate LER [C]	2.4	1.8	1.4	1.0			
Metal LWR [C]	3.9	2.7	1.8	1.5	0.9	0.9	0.9

Source: ITRS 2.0, 2015, Lithography Section, http://www.itrs2.net/itrs-reports.html

Market estimations

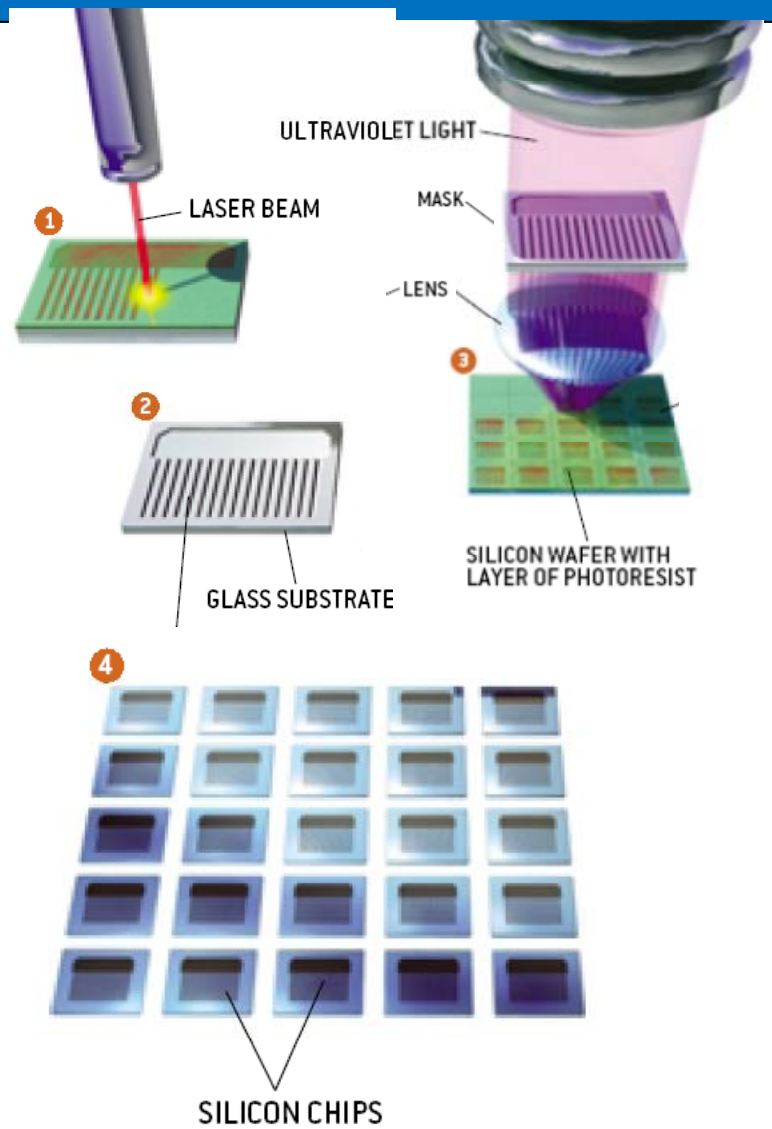


Players: Intel, Samsung, TSMC,.....
Changes in strategy ahead: optimizing performance at each node prior to lauch next one

http://spectrum.ieee.org/semiconductors/devices/intel-finds-moores-laws-next-step-at-10-nanometers

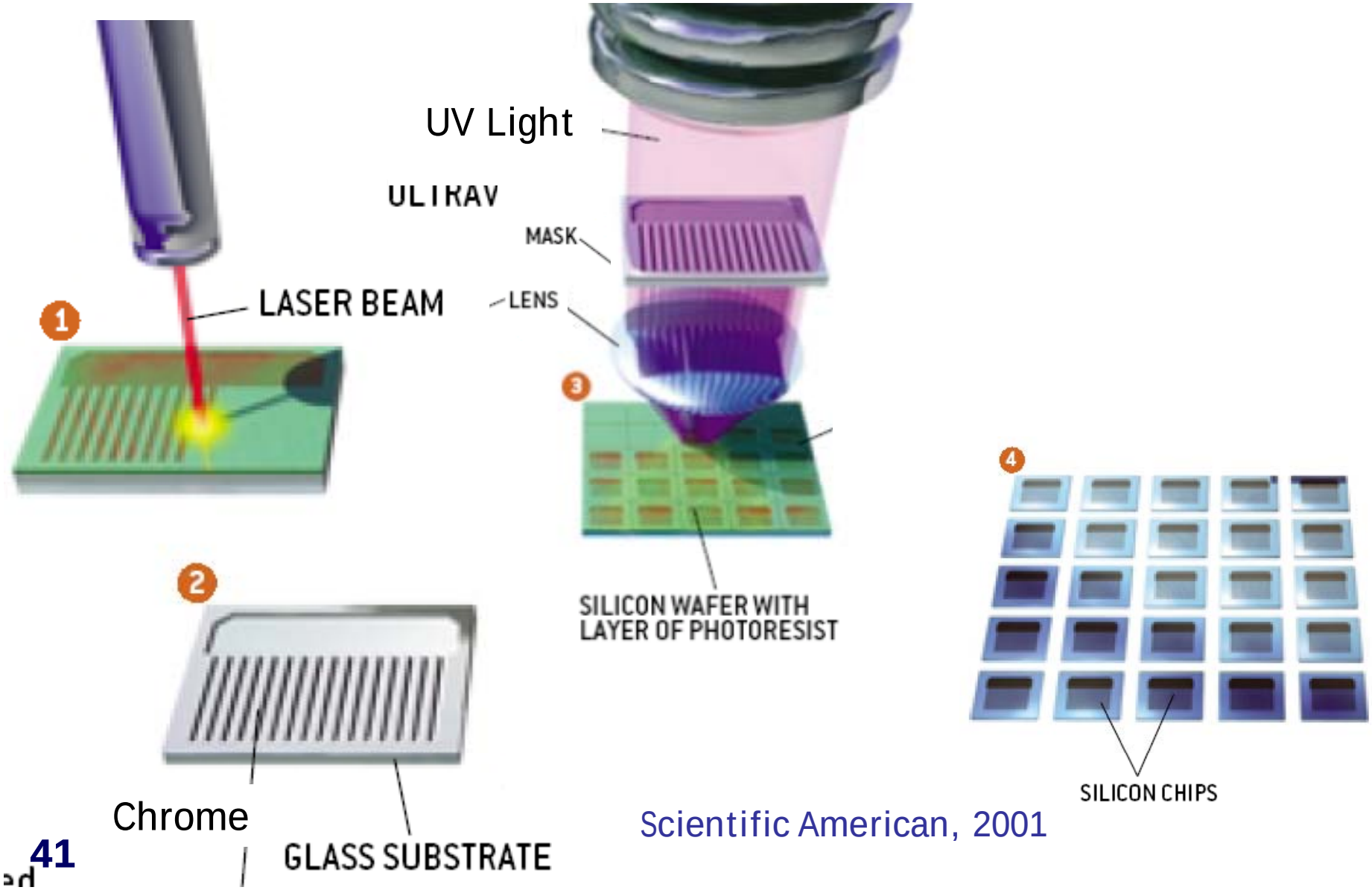
Lithography (Optical)

1. A laser beam writes the circuit pattern for a microchip on a layer of light-sensitive polymer (photoresist) that rests atop a layer of chromium on a transparent substrate (*e.g.* quartz). The sections of polymer struck by the beam can be selectively removed (developed).
2. The exposed sections of chromium are removed by etching, and the rest of the polymer is then dissolved. The result is a mask—the equivalent of a photographic negative.
3. When a beam of monochromatic ultraviolet light is directed at the mask, the light passes through the gaps in the chromium. A lens shrinks the pattern by focusing the light onto a layer of photoresist on a silicon wafer.
4. The exposed parts of the photoresist are removed, allowing the replication of the pattern in miniature on the silicon chips using etching, metal deposition, ion implantation etc.



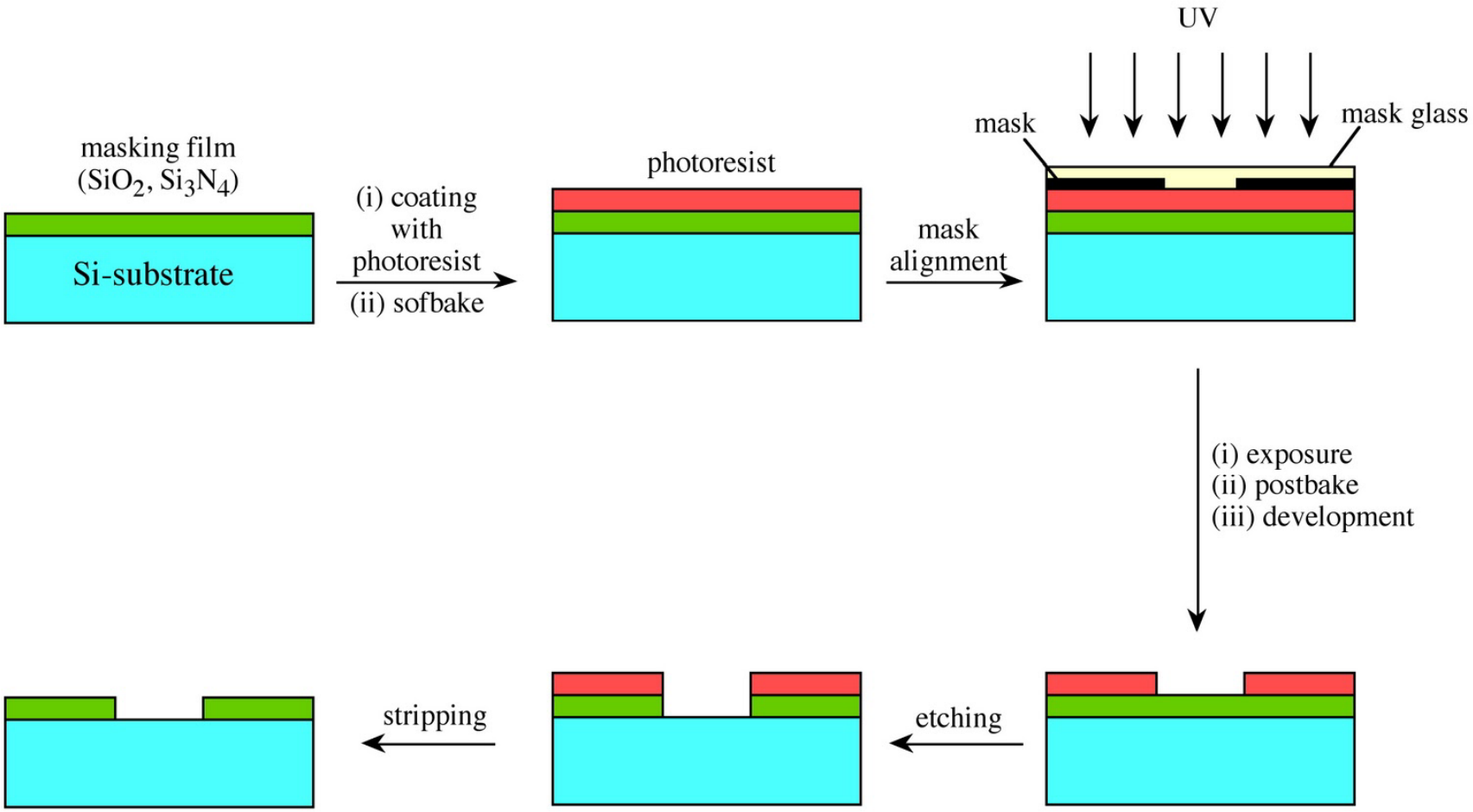
Scientific American, 2001

Optical Lithography

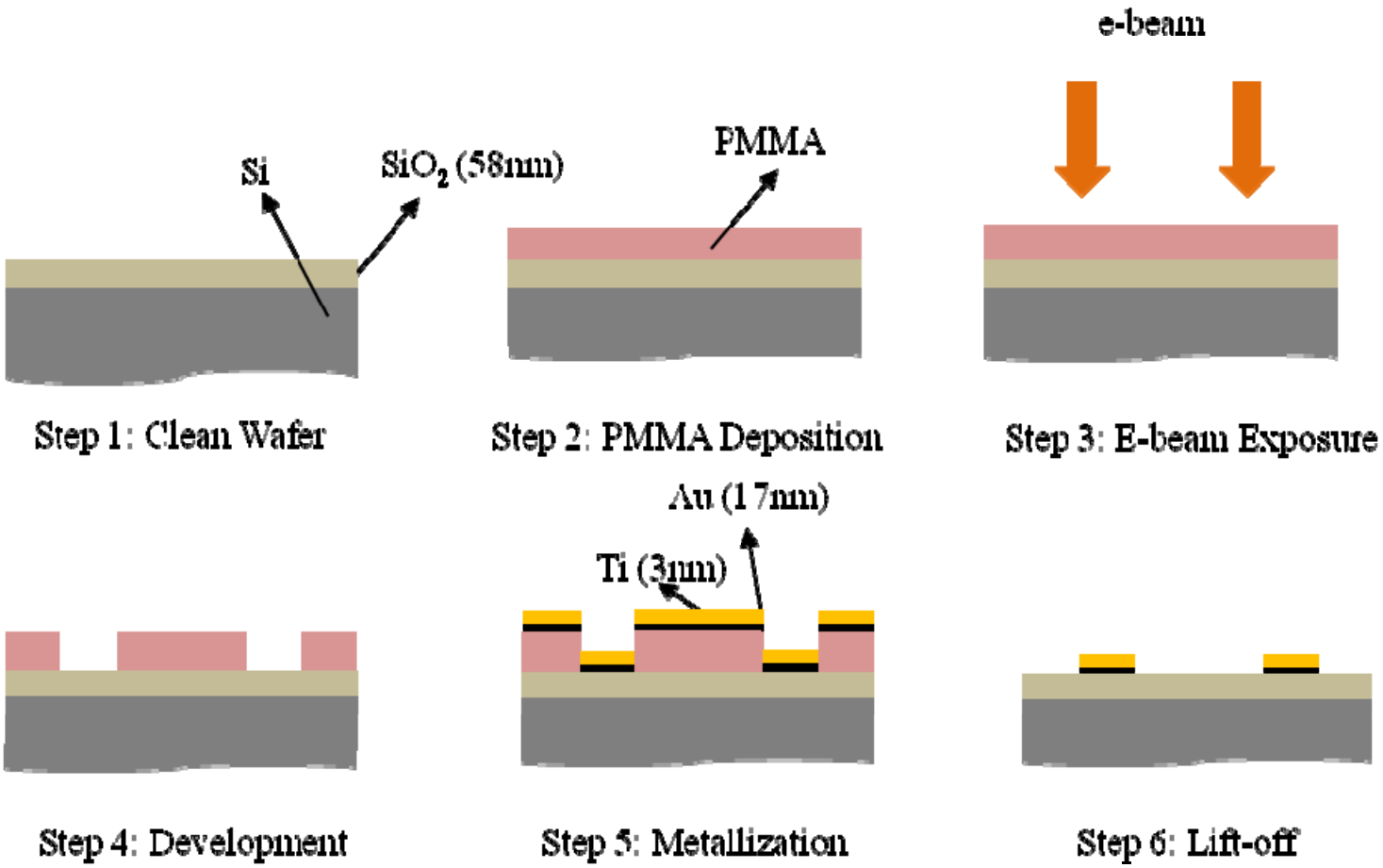


Scientific American, 2001

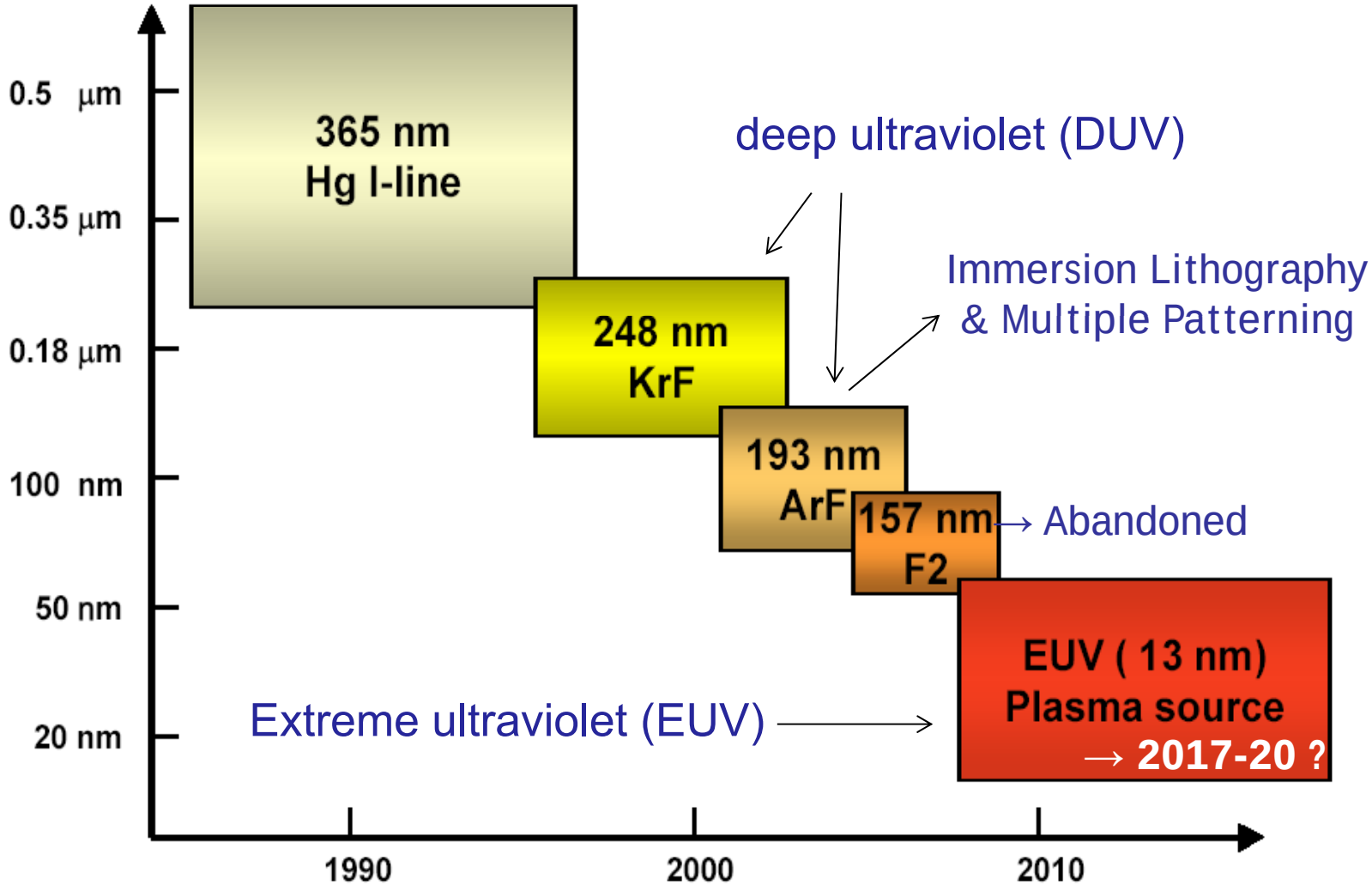
Optical Lithography



Lithography (e-beam)



Optical Lithography: Wavelengths and Sources (**NB** Historical)

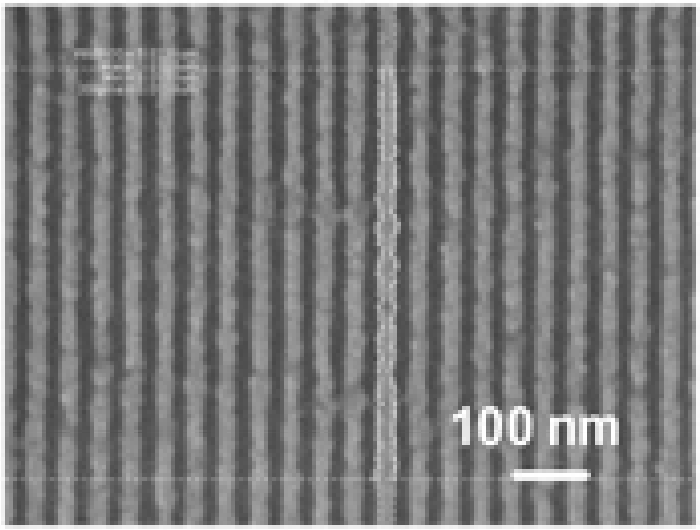


Material Challenges in Lithography

- **157nm Wavelength (never used)**
  - Photoresist
  - Quartz is no longer transparent at 157 nm - WHY (homework)
  - CaF_2 is the likely replacement material for quartz lens
  - Transparent mask pellicles (degradation)
    - Current materials fail at doses of ~10 J/cm^2
    - Goal is >1000 J/cm^2

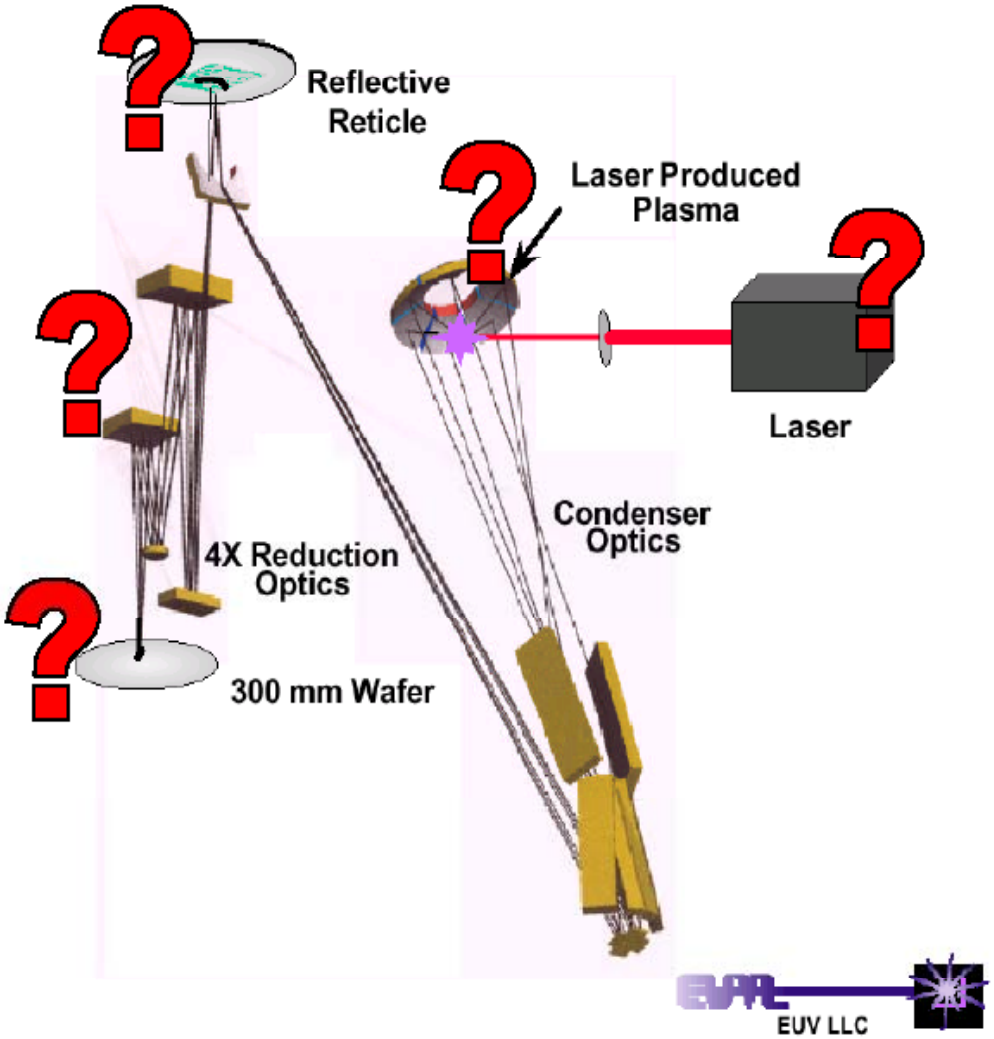
Challenges in Lithography

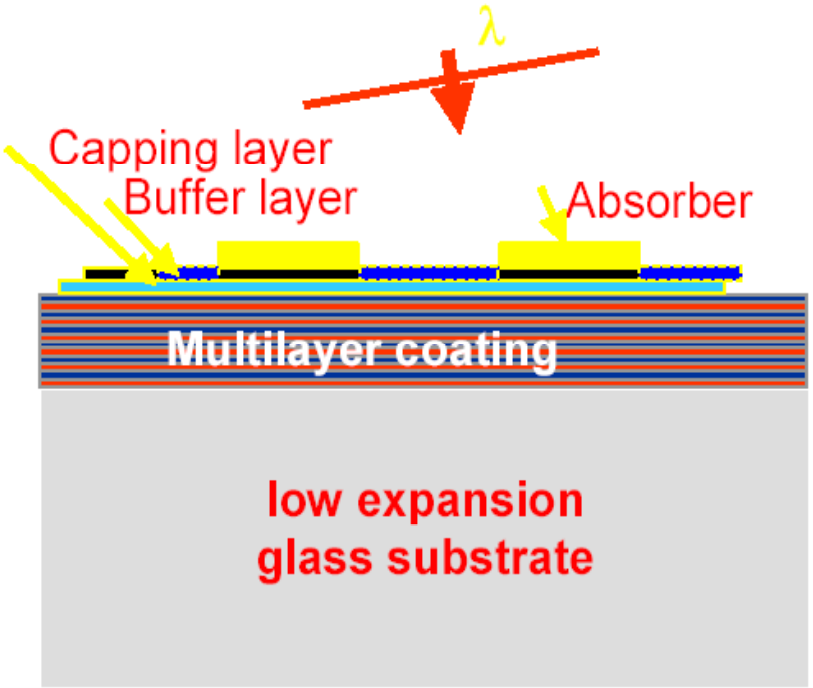
- **13nm (EUV) Wavelength (**cf. ITRS 2011 Litho Section**)**
  - Source power, source lifetime
  - Lens and mask reflective instead of refractive
  - Reflective surface is multiple alternating thin layers of Mo:Si
  - Mask defects
  - Suitable photoresist for EUV (sulfone terpolymers, truxene derivative)



SEM image in 22nm line pattern

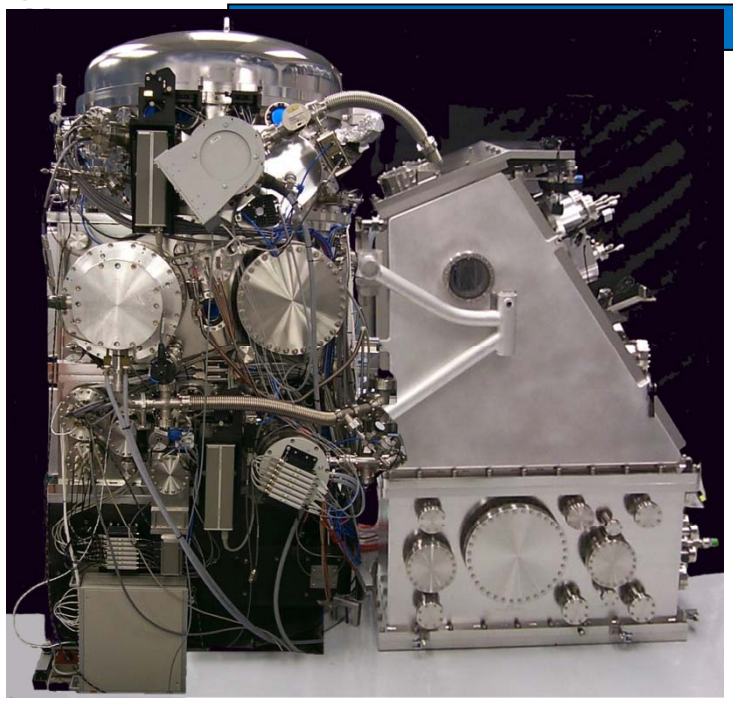
EUV: **Reflective** Optics





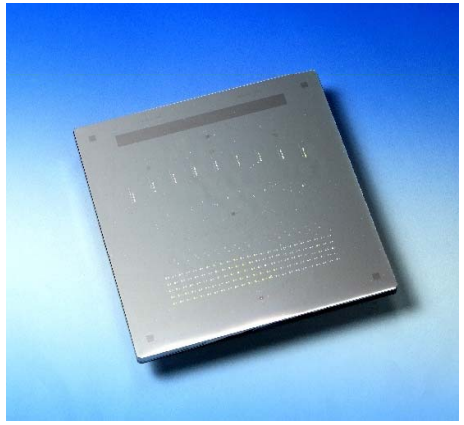
EUV Mask (UC Berkeley)

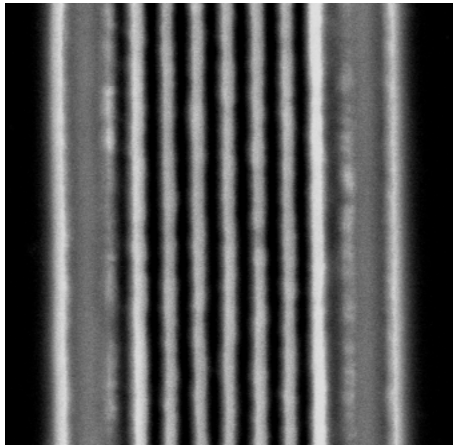
EUV Lithography: 13nm



EUV Stepper Prototype

Mask

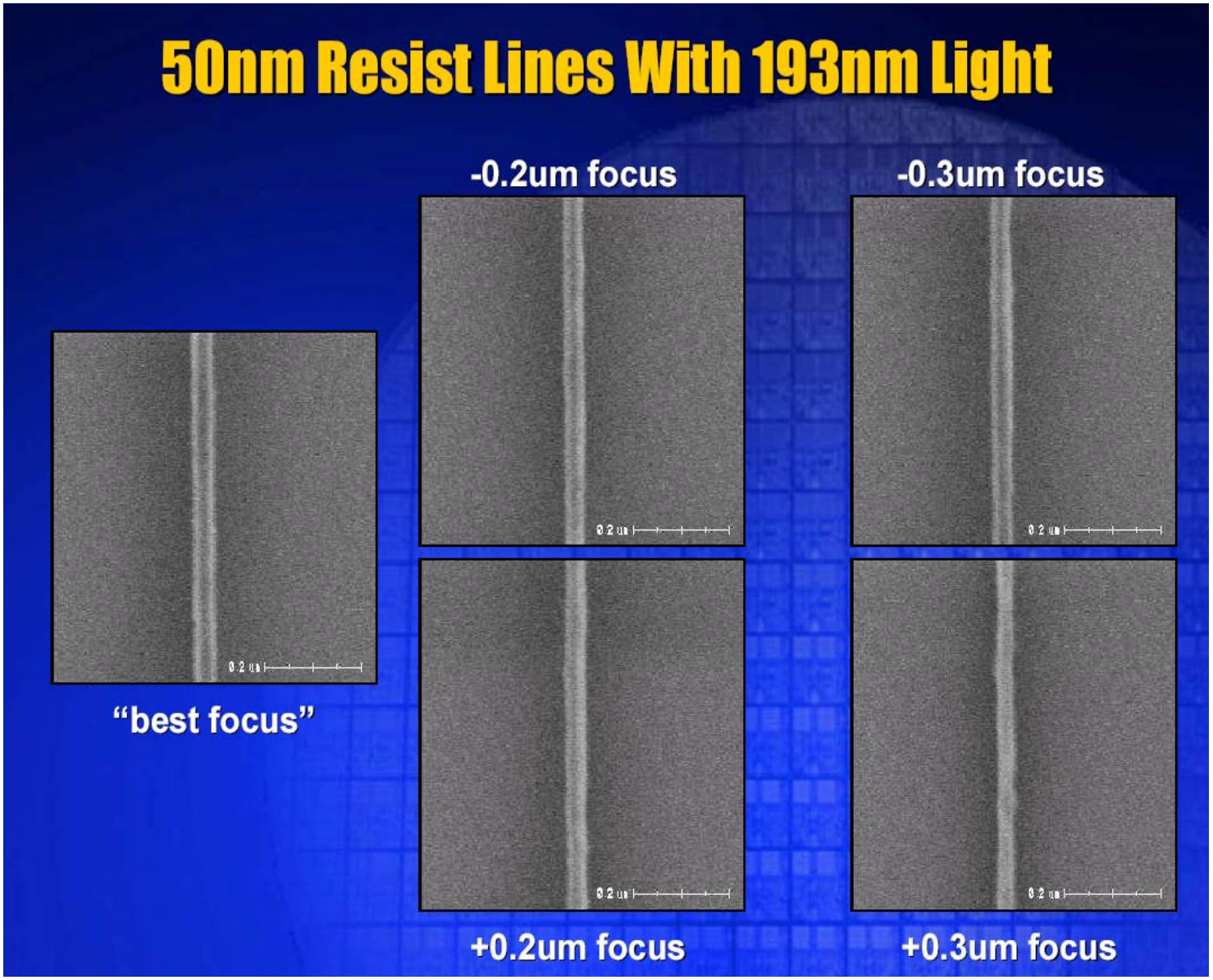




50nm Lines Printed with EUV Lithography

All Optical Elements Must Reflect 13nm Radiation

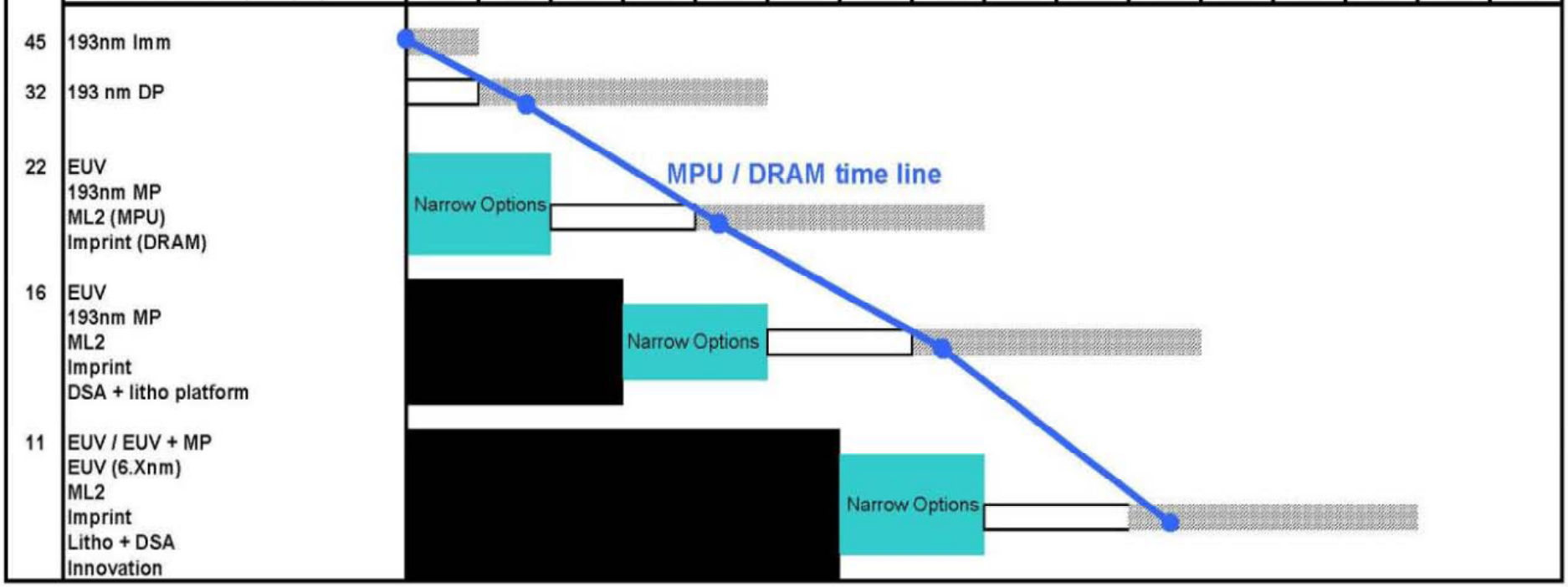
Source: Intel



Source: Intel

Lithography Technology (ITRS 2011 Lithography Chapter)

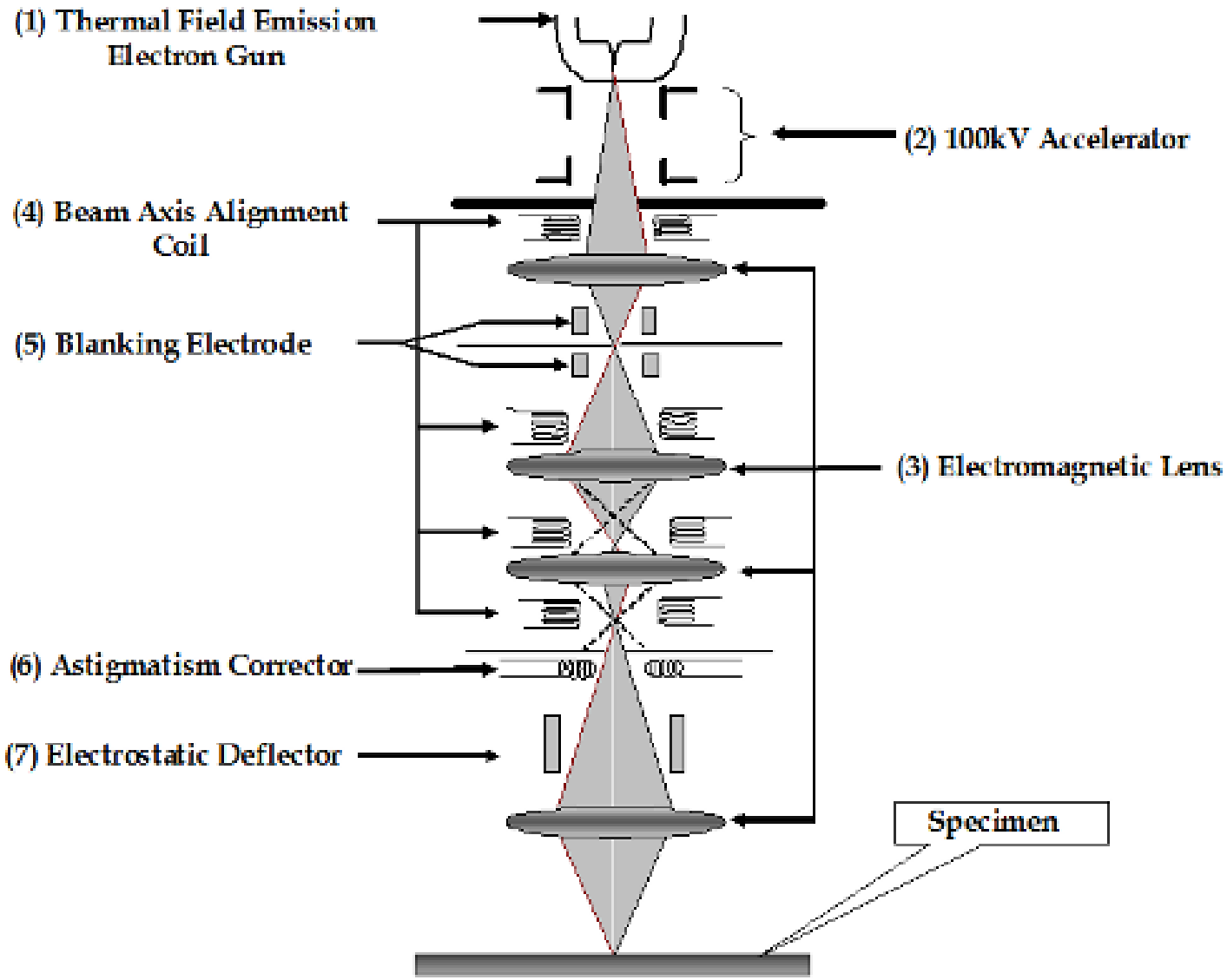
First Year of IC Production	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026
DRAM ½ pitch (nm) (contacted)	36	32	28	25	23	20.0	17.9	15.9	14.2	12.6	11.3	10.0	8.9	8.0	7.1	6.3
MPU/ASIC Metal 1 1/2 pitch (nm)	38	32	27	24	21	18.9	16.9	15.0	13.4	11.9	10.6	9.5	8.4	7.5	7.5	7.5



This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.

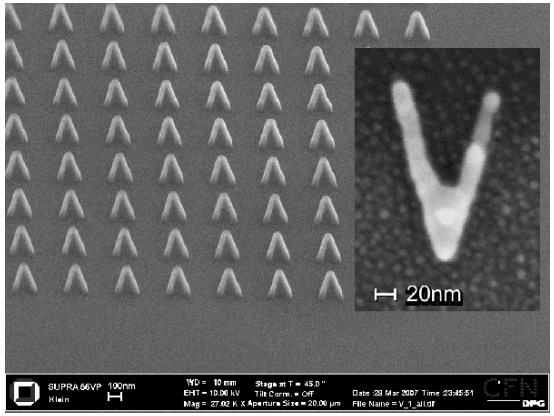
Research Required
Development Underway
Qualification / Pre-Production
Continuous Improvement

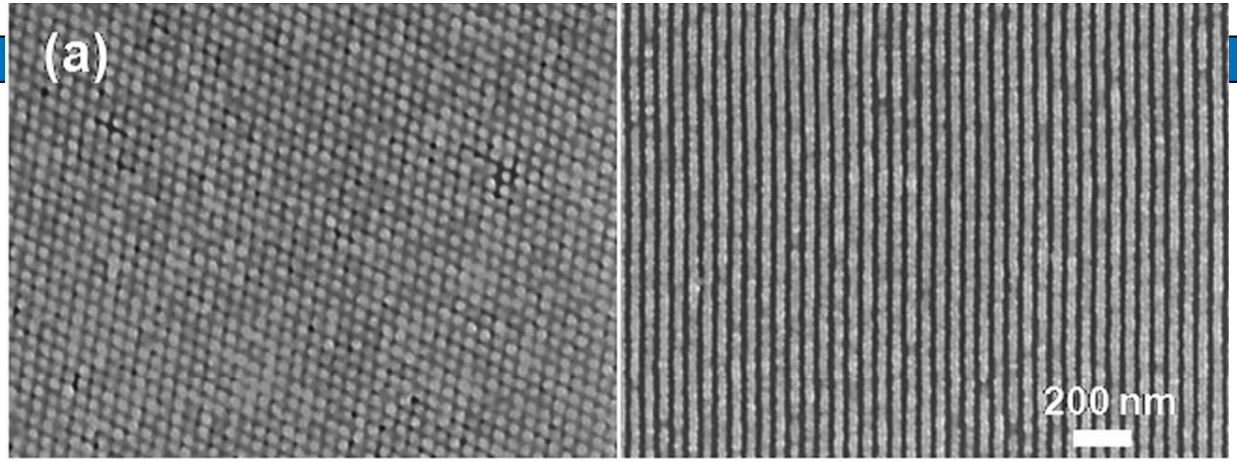
E-beam lithography

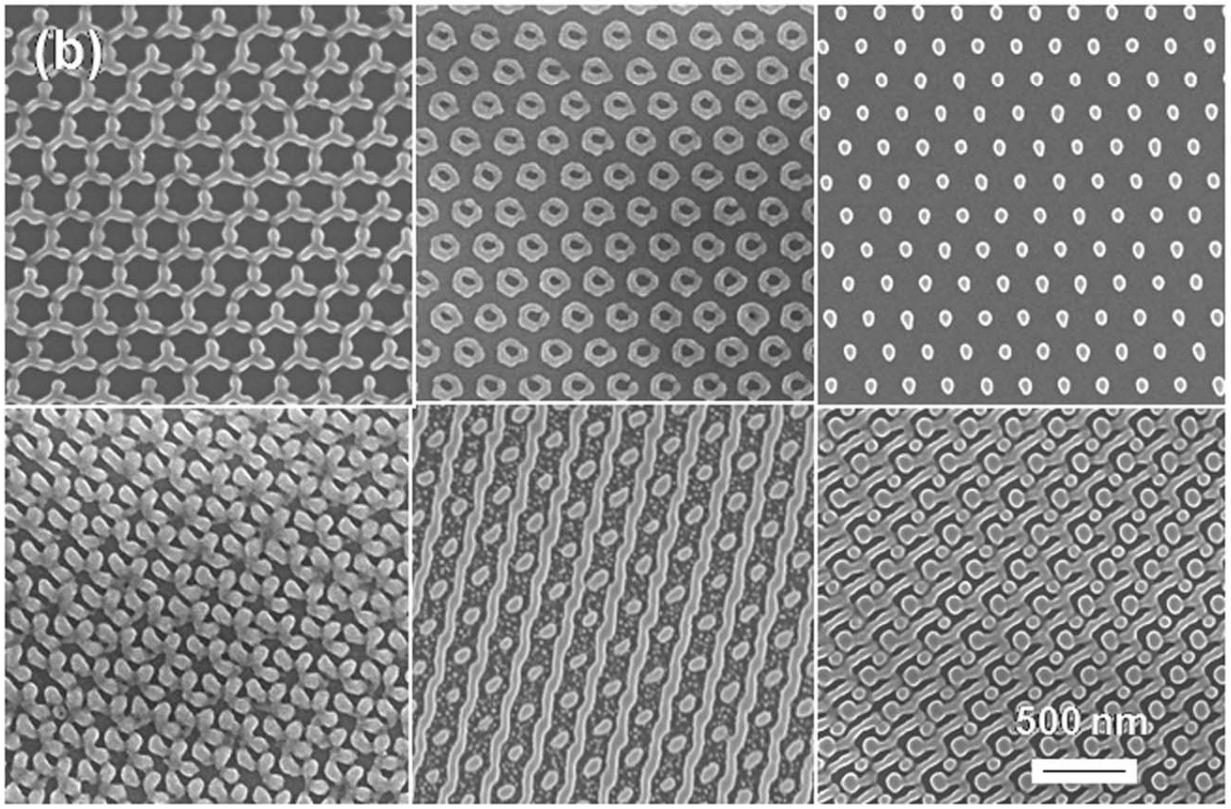


E-beam lithography

Down to 10 nm resolution

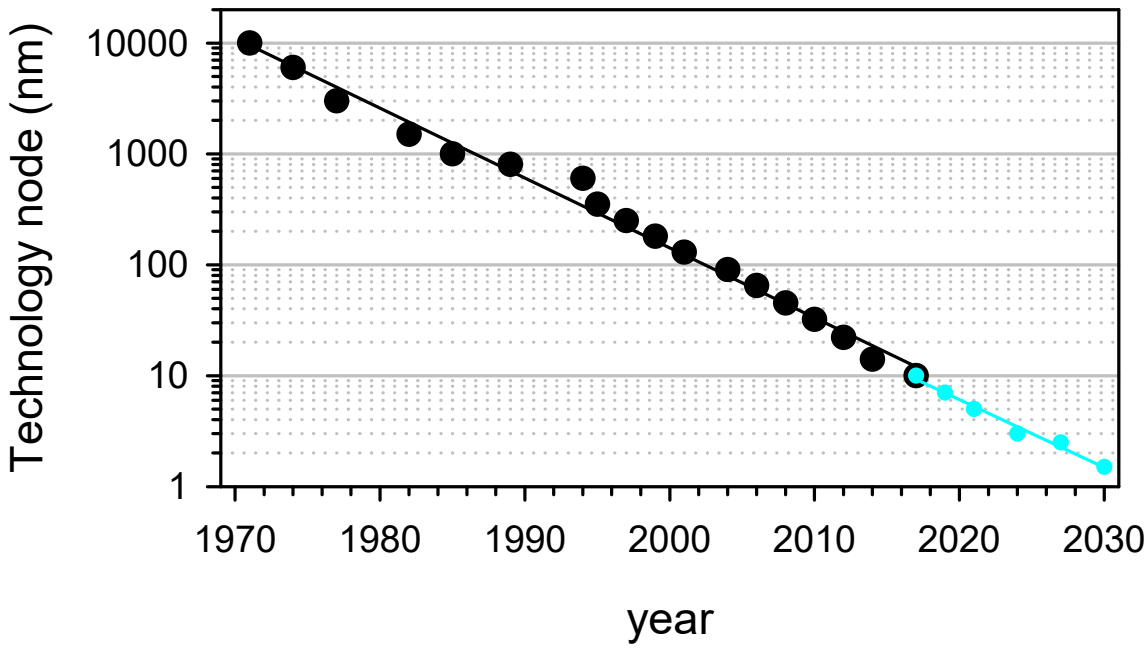






Moore's Law driven by scaling

All leading-edge logic products:



Source: ITRS 2015

Complementary Metal-oxide Semiconductor (CMOS) Technology Roadmap

"Classical" CMOS: "the same only smaller (and faster)"

Non-classical CMOS

- SOI (Silicon on Insulator)
- Si/SiGe
- High-K dielectrics (2007)

Feature sizes ~ 100 nm
Intel Fab 24, Leixlip

New Technologies

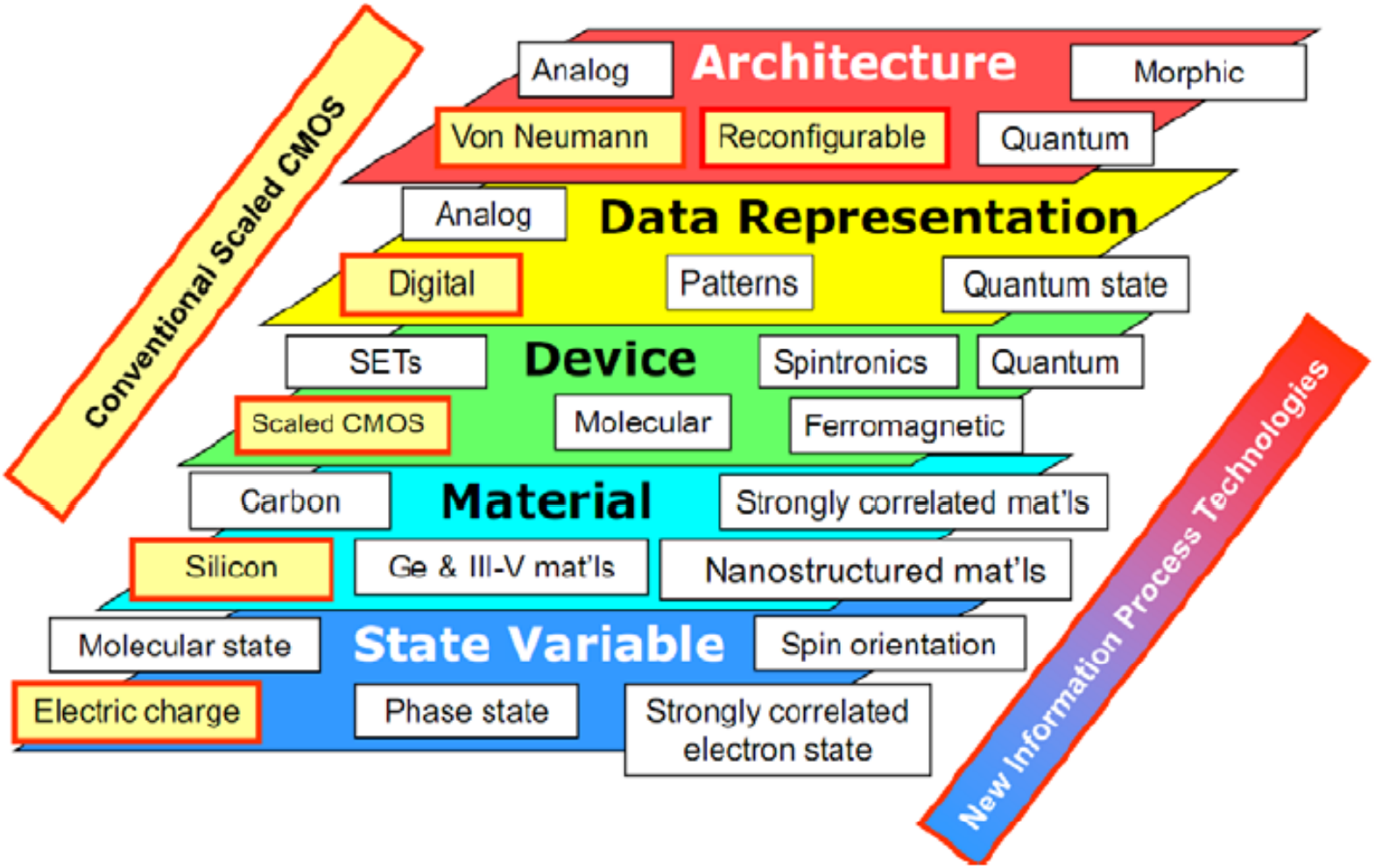
- Quantum devices
- Spin-electronics
- Molecular electronics
- Quantum Computing

2004 2006 2008 2010 2012 2014 2016 2018

sizes~10 nm

- Near term: Develop manufacturable non-classical or hybrid alternatives to CMOS
- Long term: Invention a feasible new information and signal processing technology addressing "beyond CMOS" applications

Taxonomy for Nanoscale Information Processing

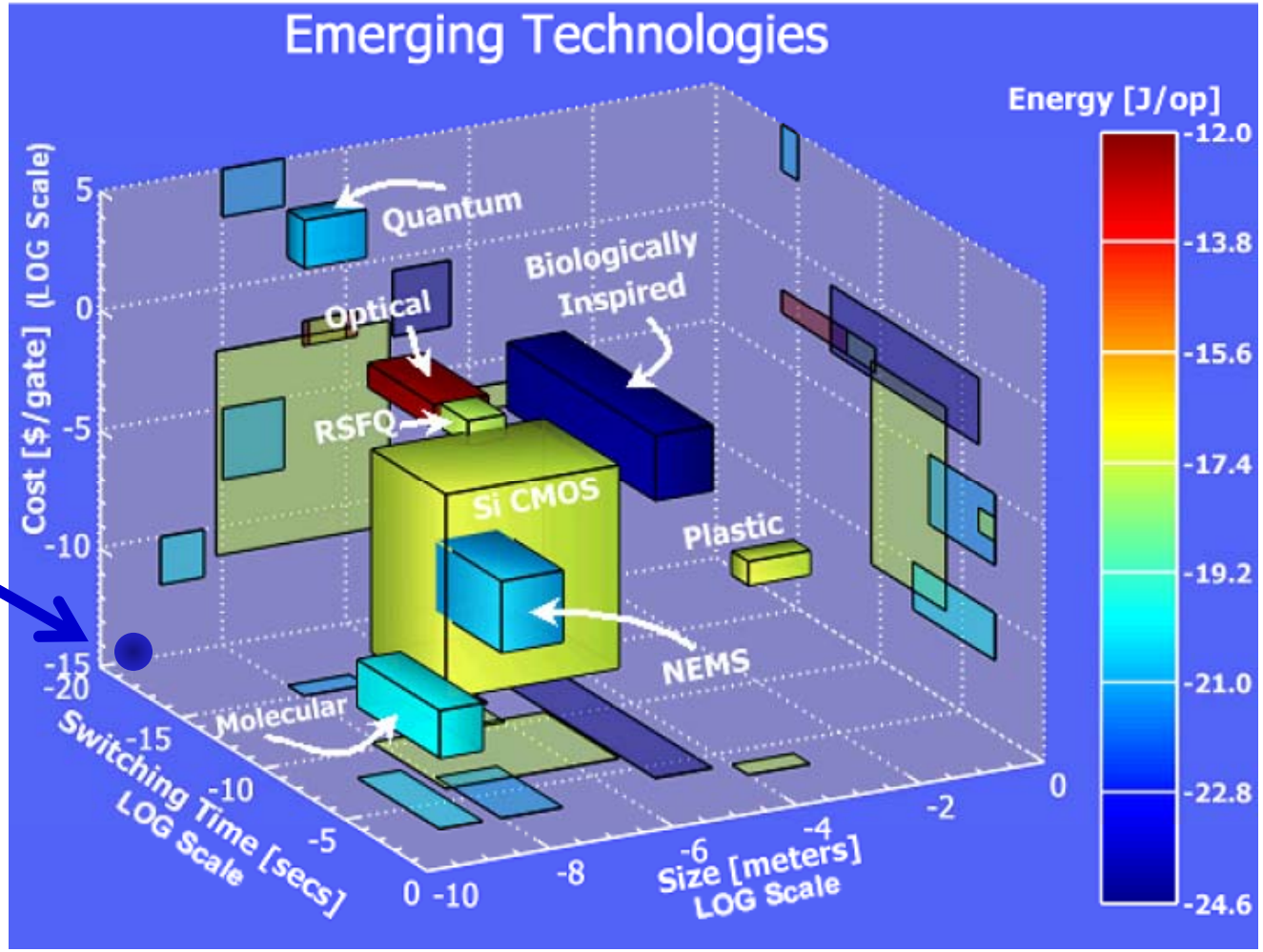


Source: International Technology Roadmap for Semiconductors 2009

Information Processing & Storage in the 21st Century: Speed, Size, Cost, Power Consumption

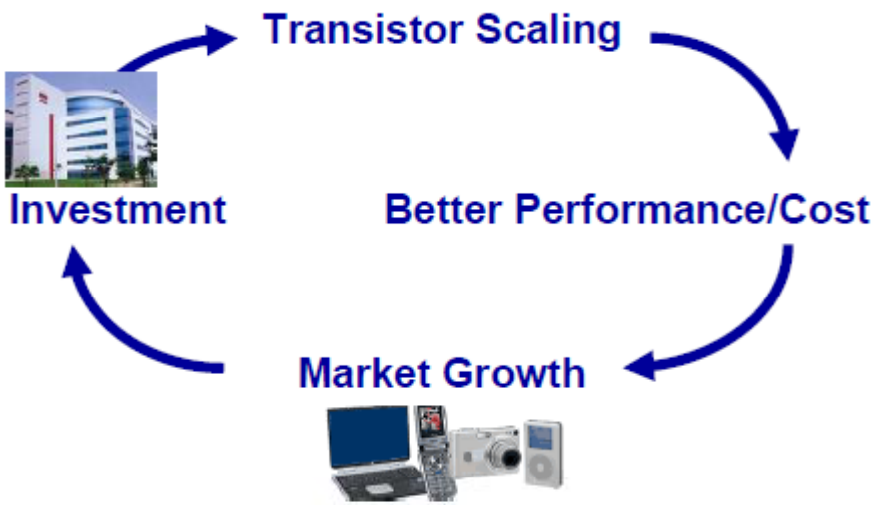
Estimated Parameters for Emerging Research Devices and Technologies in 2016

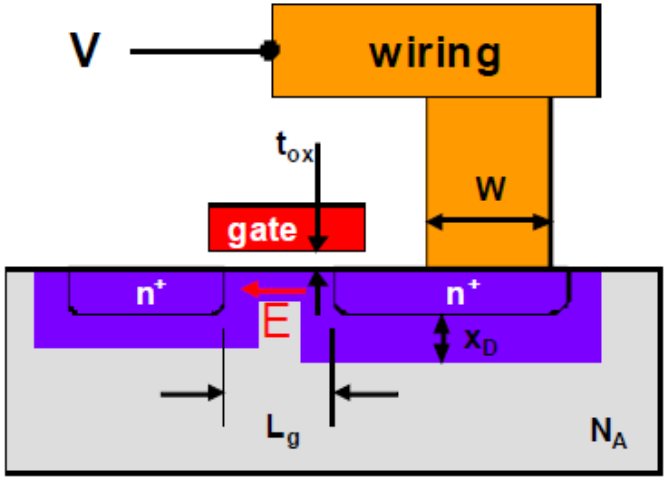
"Perfect":
Small
Fast
Cheap
Low-Power



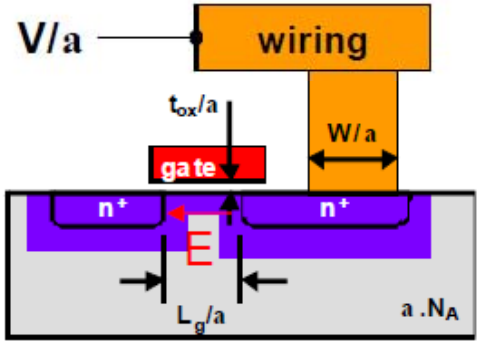
Source: ITRS 2005

Why Scaling ?





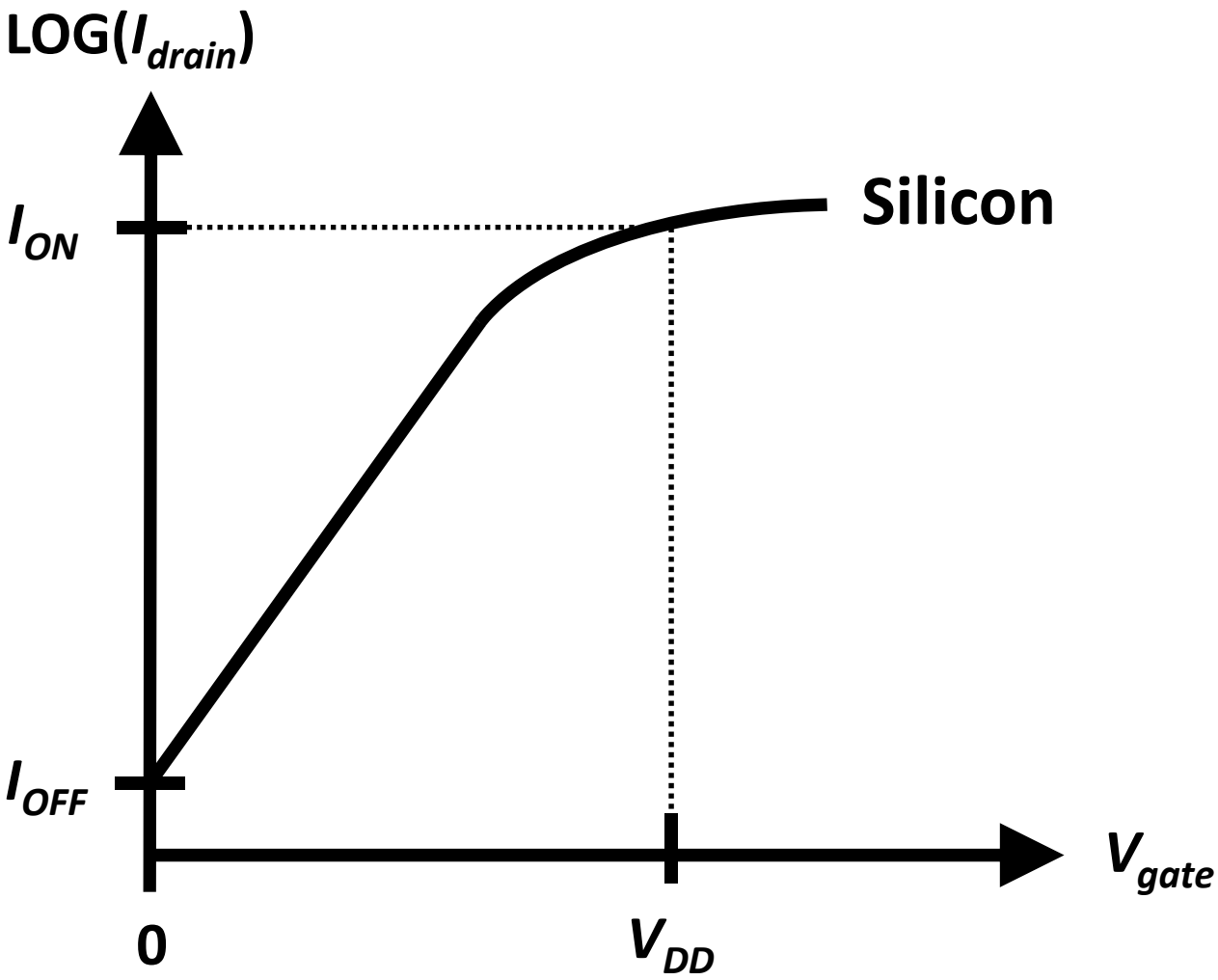
dimensions t_{ox}, L, W	1/a
doping	a
voltage	1/a
integration density	a^2
delay	1/a
power dissipation/Tr	$1/a^2$
Electric Field E	1



Constant field scaling (1960-2003). Theory predicts increased speed and lower power consumption of digital MOS circuits when the critical dimensions are scaled down.

Dynamic Power Dissipation

→ Scaling Supply Voltage (V_{DD})



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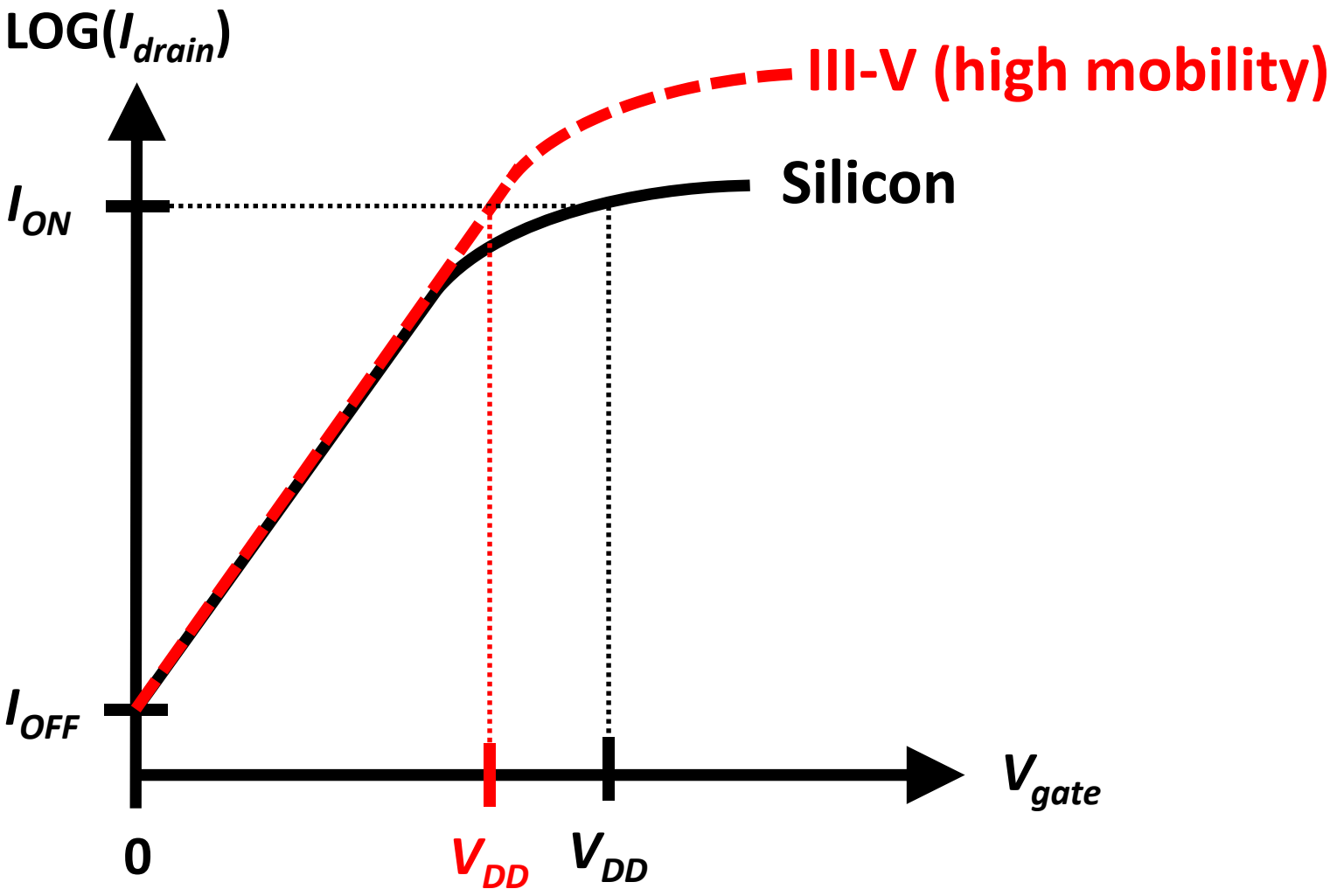
Dynamic Power Dissipation

→ Scaling Supply Voltage (V_{DD})



V_{DD} = V_{GS} at the current settled as "on"

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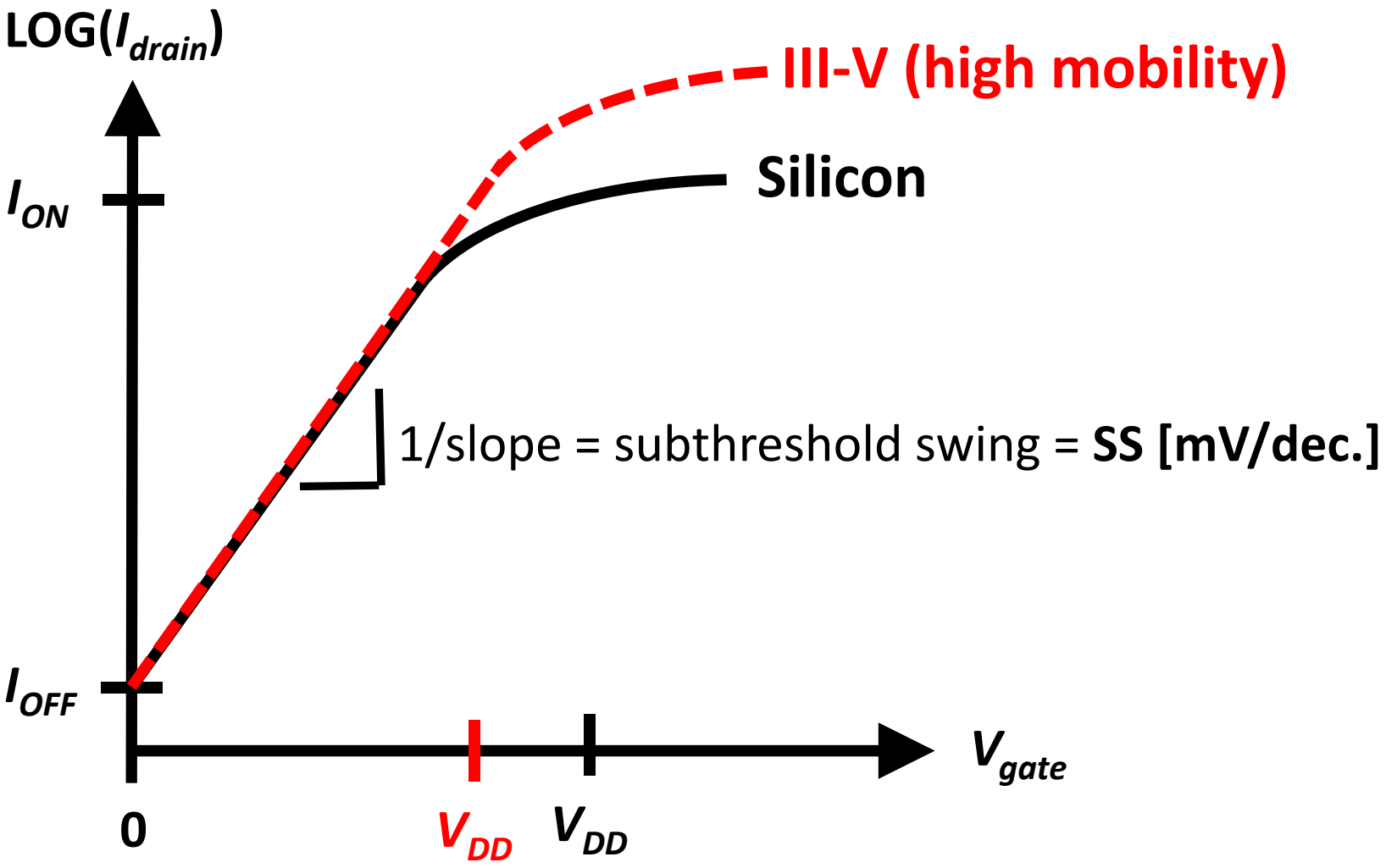
Dynamic Power Dissipation

→ Scaling Supply Voltage (V_{DD})



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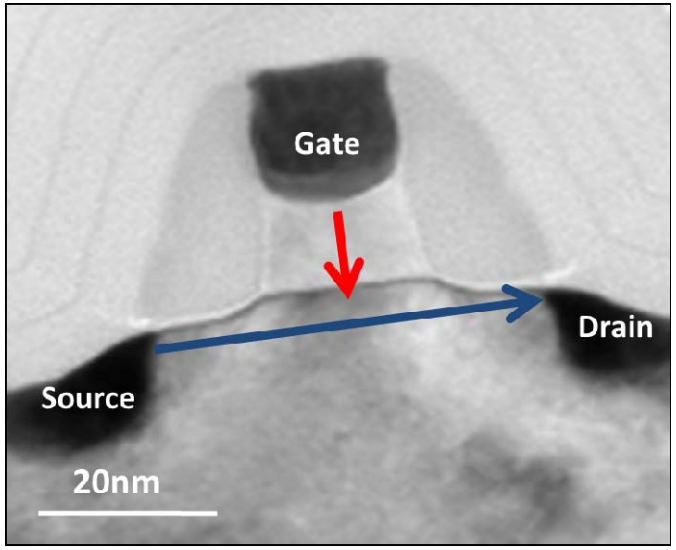
Total Power Dissipation in CMOS Circuitry

$$P_{total} = P_{dynamic} + P_{static}$$

Leakage

Charging/discharging load capacitance



61

Dynamic Power Dissipation

→ Scaling Supply Voltage (V_{DD})

$$P_{dynamic} = C_{load} \cdot V_{DS}^2 \cdot f$$

$$I_{DS} = \mu \cdot C_{ox} \cdot (w/L) \cdot (V_{GS}-V_{Th}) \cdot V_{DS}$$

L and w, length and width of the channel, C_{ox} capacitance of insulating layer, V_{GS} , V_{Th} and V_{DS} voltage gate-source , threshold (V_{DD}) and drain-source

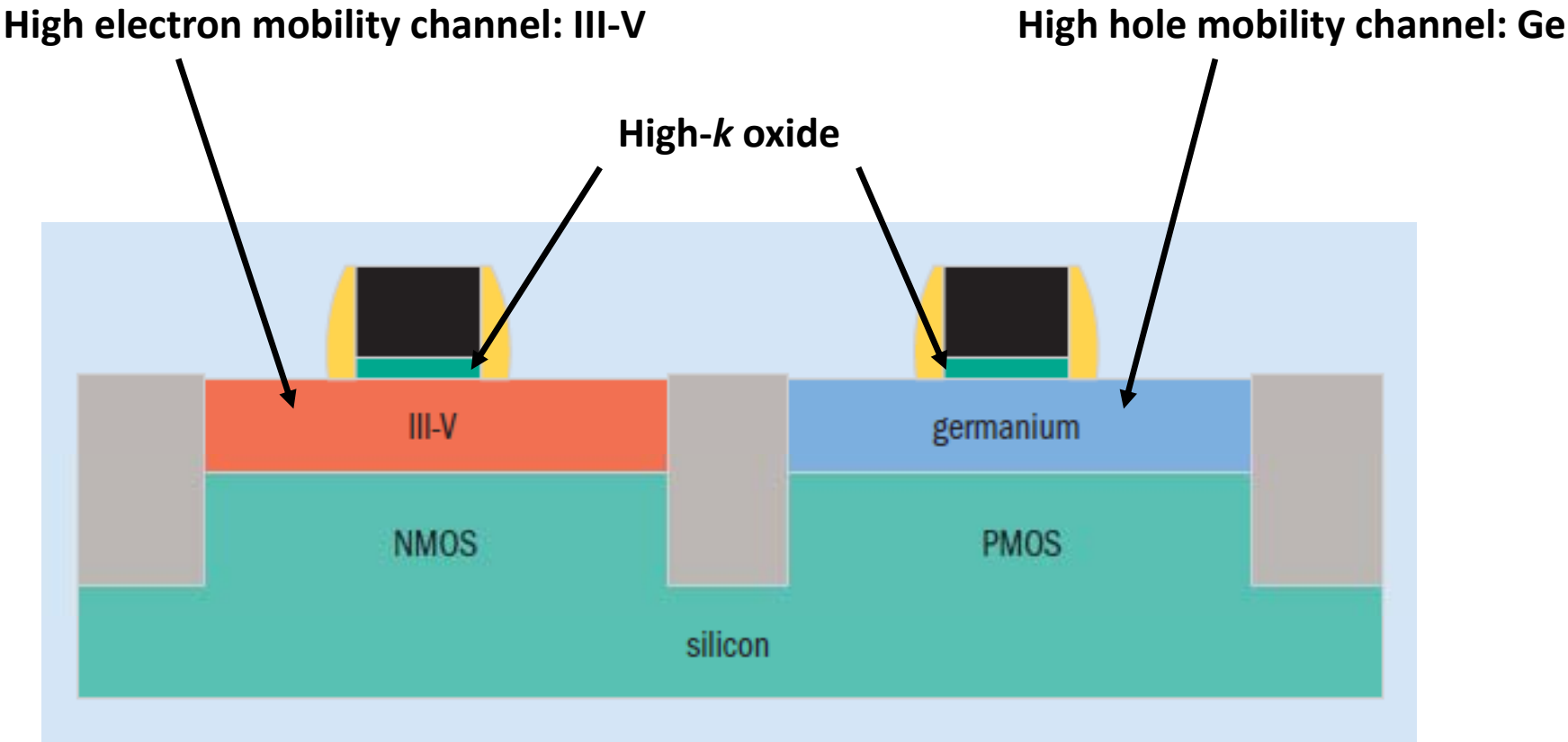
Introduce high mobility materials to reduce V_{DS}

Material	Si	Ge	GaAs	$In_{0.53}Ga_{0.47}As$	InAs	InSb
Electron Mobility (cm^2/Vs)	1400	3900	8500	14000	40000	78000
Hole mobility (cm^2/Vs)	450	1900	400	300	500	850

62

The holy grail !

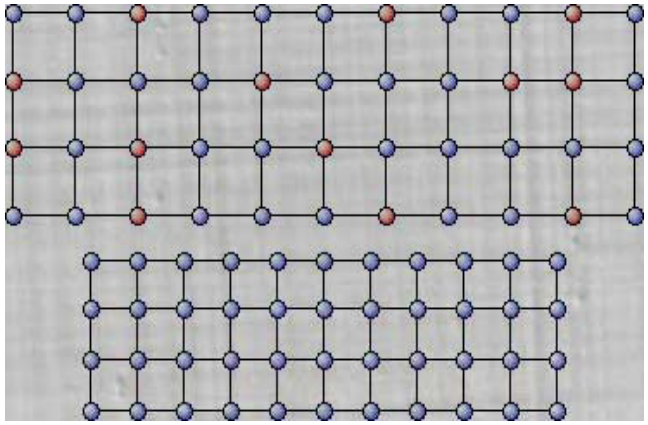
Monolithic integration of high-*k*/III-V and high-*k*/Ge on Si



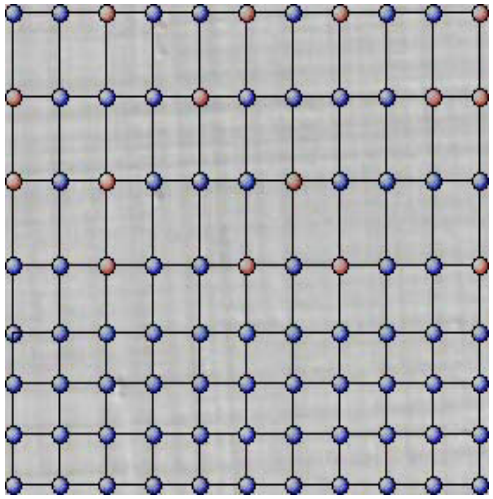
63

Strained Silicon
Heteroepitaxy – e.g. Growth of SiGe on Si

1

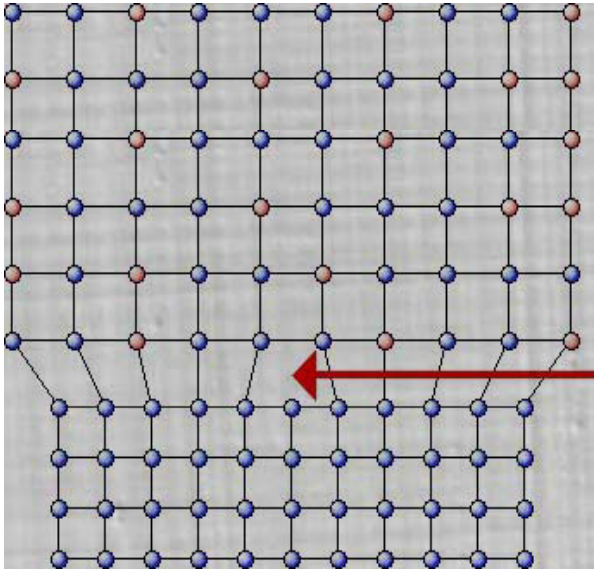


2



1. Growth of SiGe on Si (4% lattice mismatch)
2. Below a critical thickness – strained growth
3. Above critical thickness - dislocations

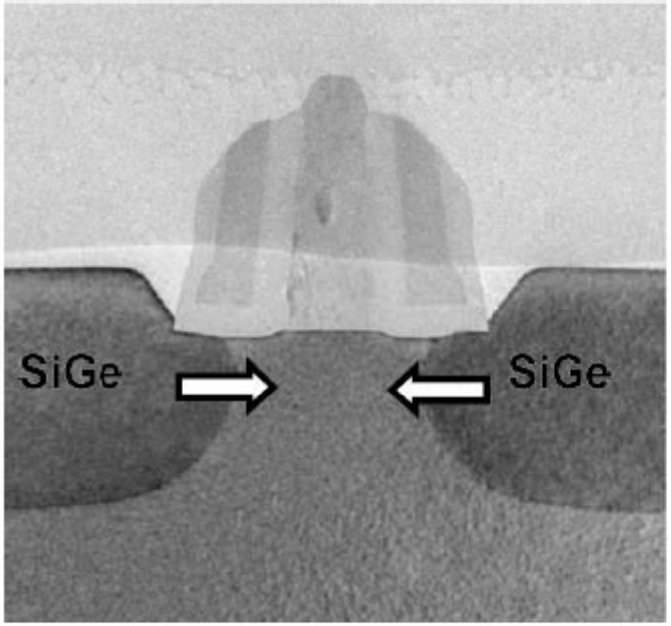
3

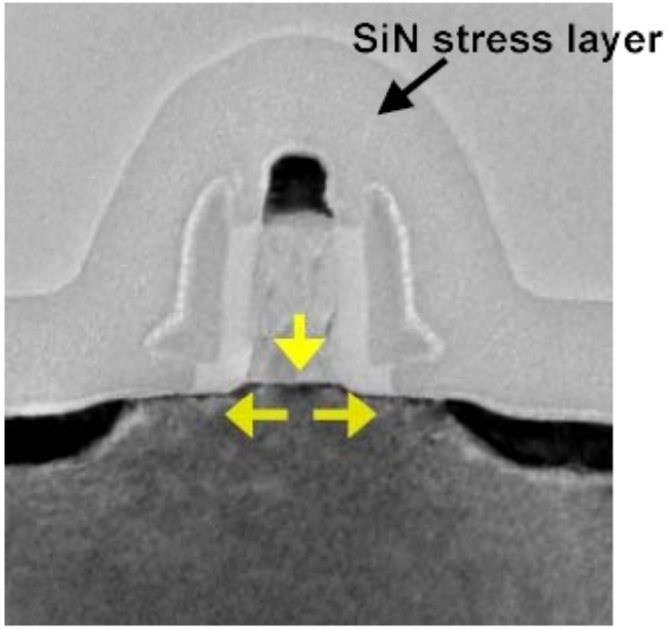


http://www.phy.cam.ac.uk/sige/content.php?pg=bg_strain

Strained PMOS and NMOS devices

PMOS T. Ghani et. al. IEDM, 2003 **NMOS**





Compressive Strain

Tensile Strain

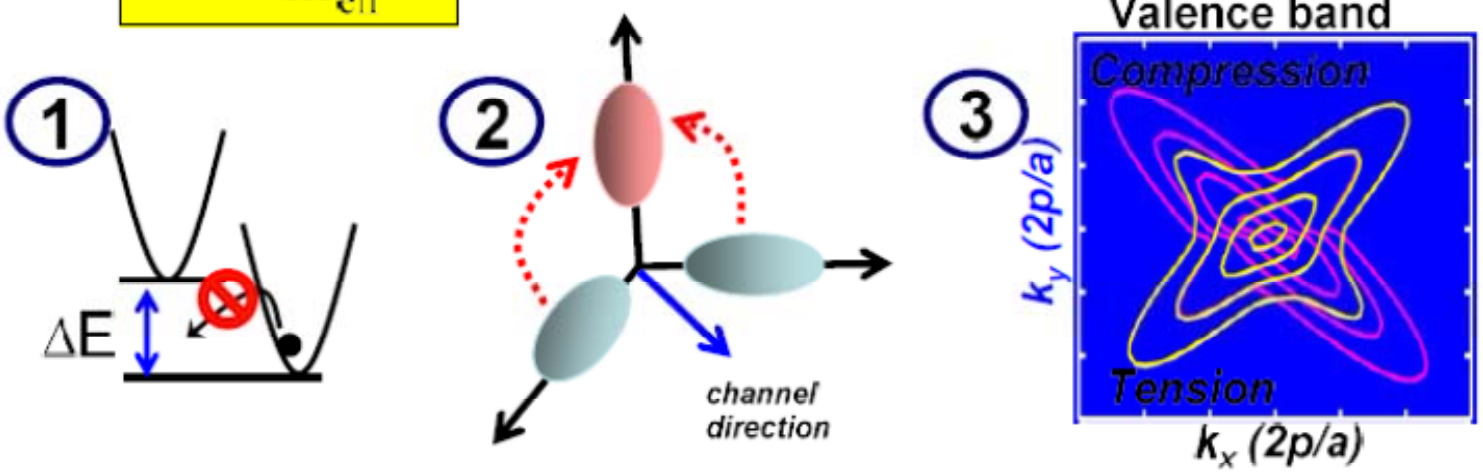
Source: Intel (Oct. 2009)

Strained PMOS and NMOS devices

Strain impacts mobility through:

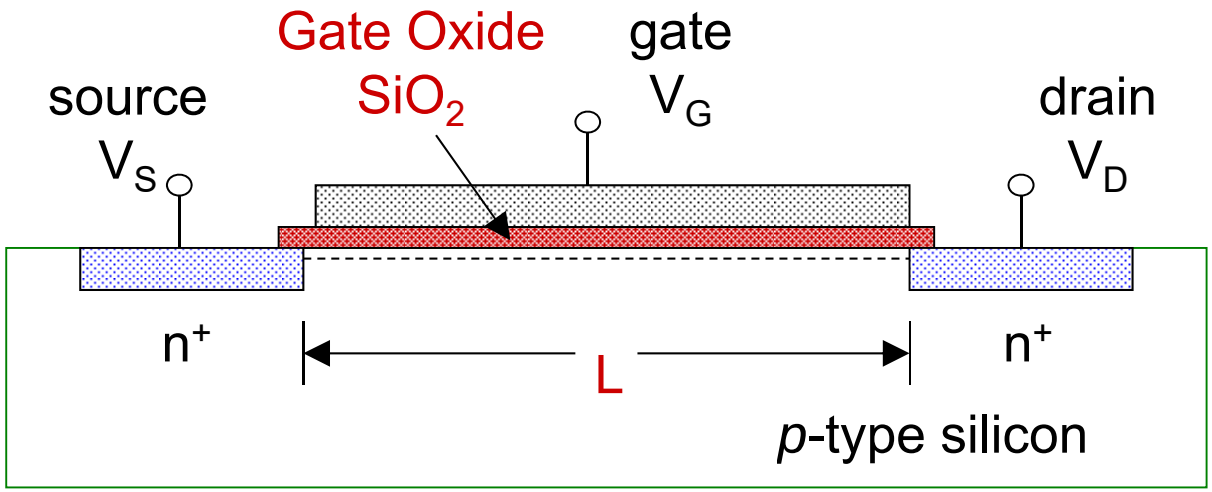
- **Energy/subband spacing which affects scattering (τ)** (1)
- **Valley repopulation which changes transport mass (m_{eff})** (2)
- **Band warpage which changes transport mass (m_{eff})** (3)

$$\mu = \frac{q < \tau >}{m_{eff}}$$



M. Stettler, 2006 SINANO Device Modeling School

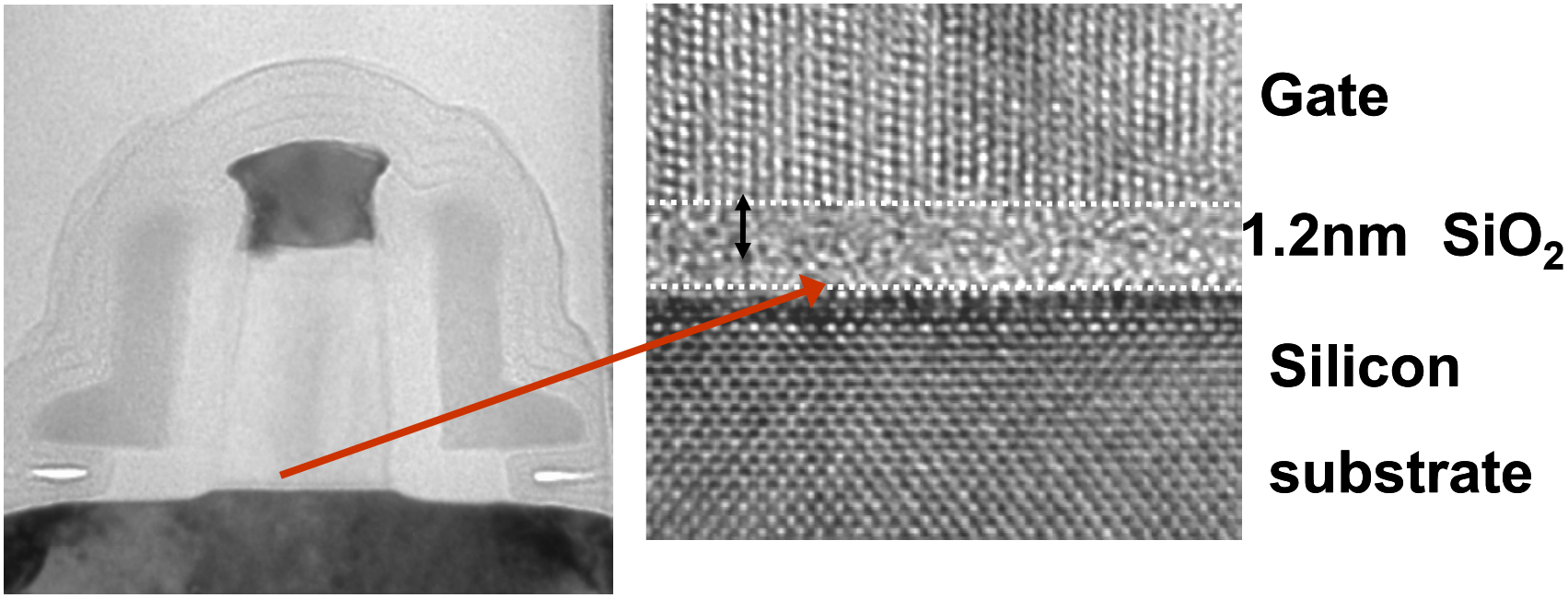
Problems with ultra-thin SiO_2 Gate Oxide layers



- At thickness 1 - 1.2 nm, excessive direct tunnelling in SiO_2
  - Leakage currents in excess of 100 A cm^{-2}
- Boron penetration through SiO_2 layer from polysilicon in *p*-channel MOSFET's, after high temperature processing
- Degenerate doped polysilicon gate electrodes
  - In inversion, polysilicon becomes depleted of carriers

Source: Barry O'Sullivan (High-K group, Tyndall)

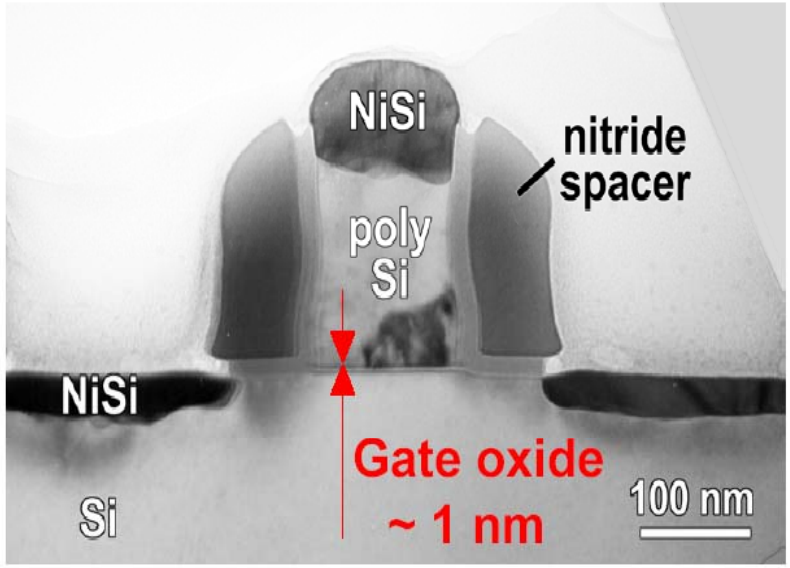
Gate oxide (dielectric)

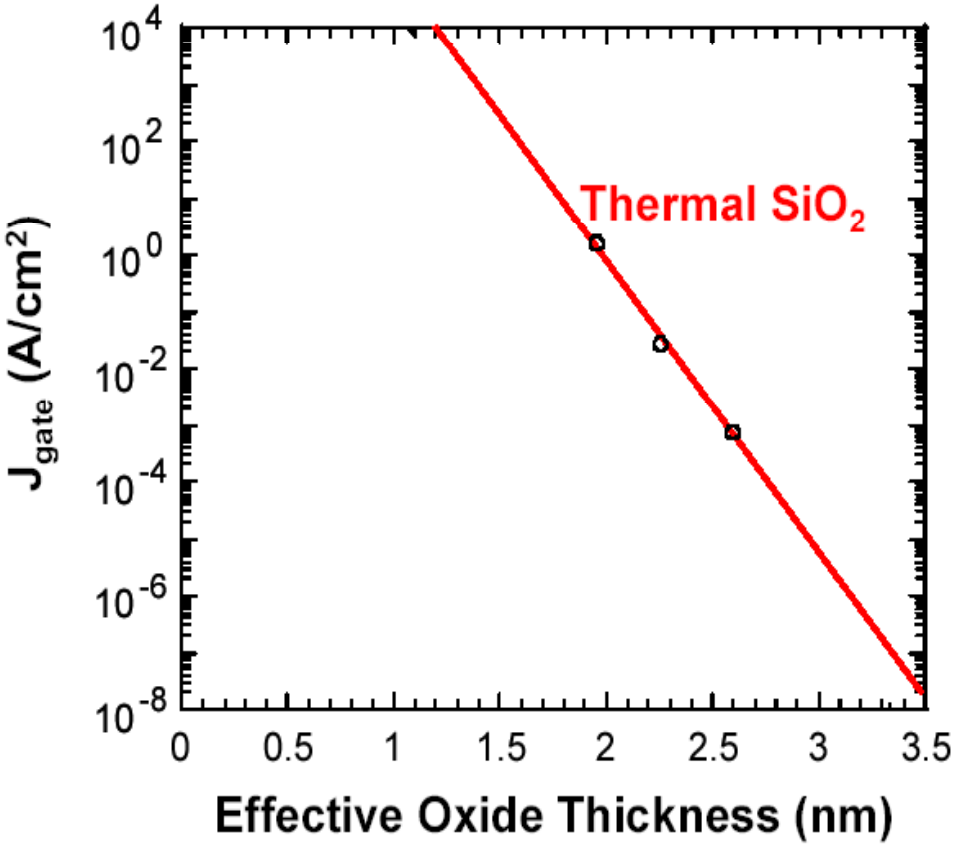


- 90 nm process
- 1.2 nm gate oxide thickness = 5 atomic layers
- Current Leakage is a Serious Problem

Source: Intel

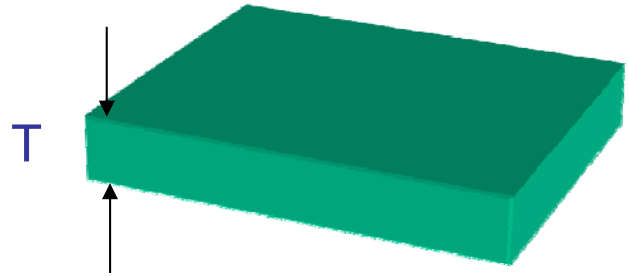
Gate Leakage Currents





Solution: High-*K* (κ) Gate Dielectric

$$\frac{C}{A} = \frac{\varepsilon_0 \kappa}{T}$$



C: Capacitance *A*: Area *K* (κ): Dielectric Constant

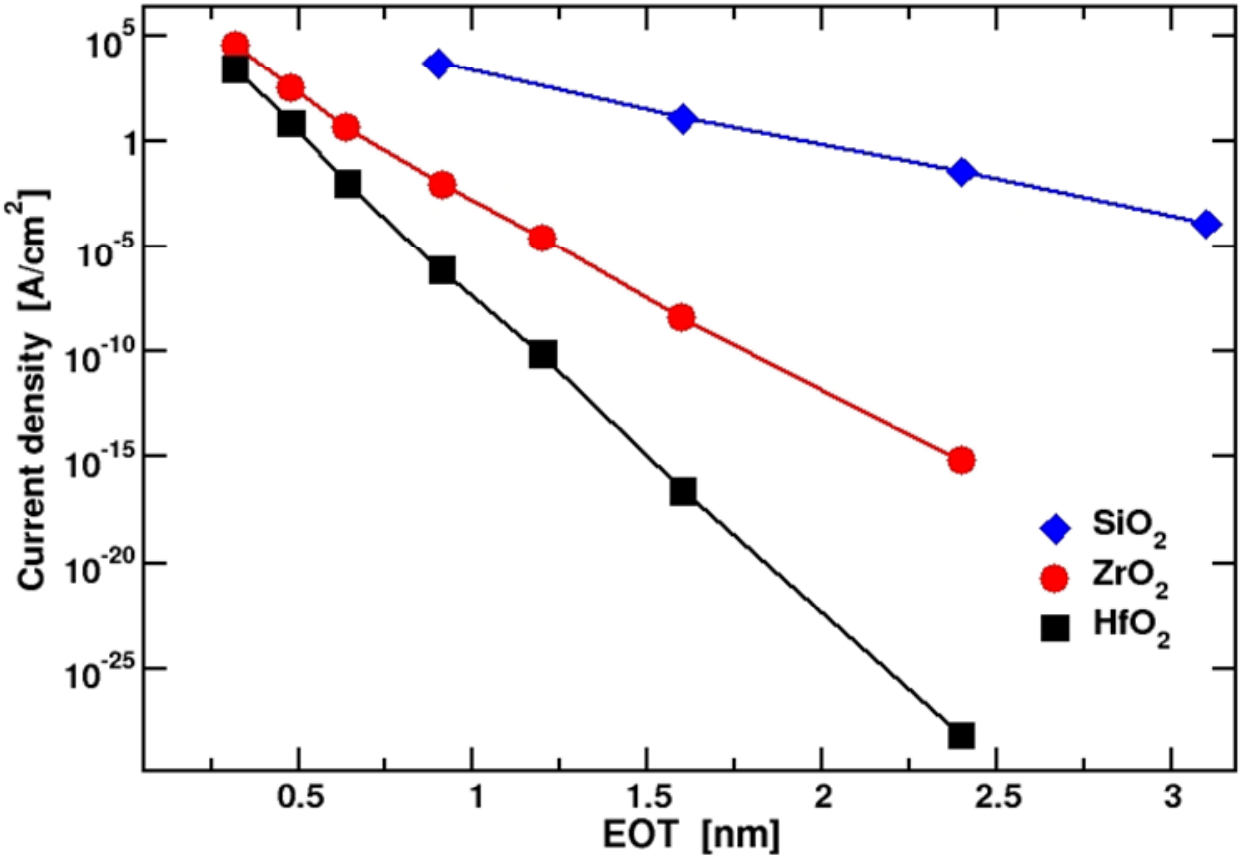
T: Thickness (physical)

Effective/Electrical Oxide (SiO_2) Thickness (EOT) = T × K_{SiO2} / *K*

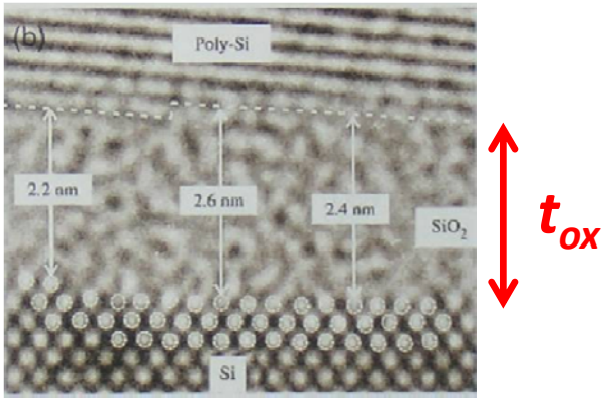
- If material with higher permittivity is introduced, increase thickness to get same capacitance per unit area
  - As layer is physically thicker, reduced tunnelling currents
- Replace polysilicon electrodes with metal electrodes
  - Can ensure adequate band offsets for both *n* and *p*-MOS devices

Solution: High-*K* (κ) Gate Dielectric

Effective/Electrical Oxide (SiO_2) Thickness (EOT) = T × K_{SiO2} / *K*



http://www.tibercad.org/sample_application/article/multiscale_simulation_mosfets_based_high_k_oxides



Oxide thickness scaling

-> increased gate leakage

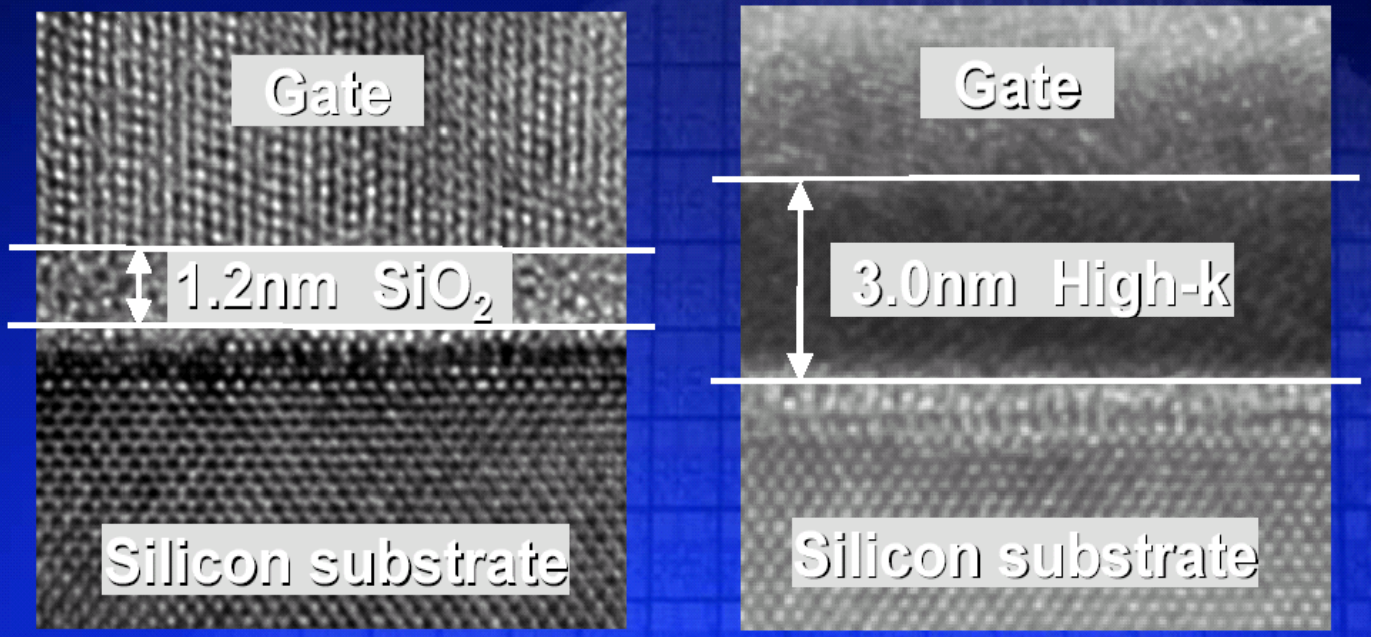
$$P_{static} = I_{leakage} \cdot V_{DD}$$

$$I_d = \mu \cdot C_{ox} \cdot (W/L) \cdot (V_g - V_T) \cdot V_{ds}$$

$$C_{ox} = \varepsilon_0 \cdot k / t_{ox}$$

Introduce high-*k* materials to increase t_{ox}

High K for Gate Dielectrics

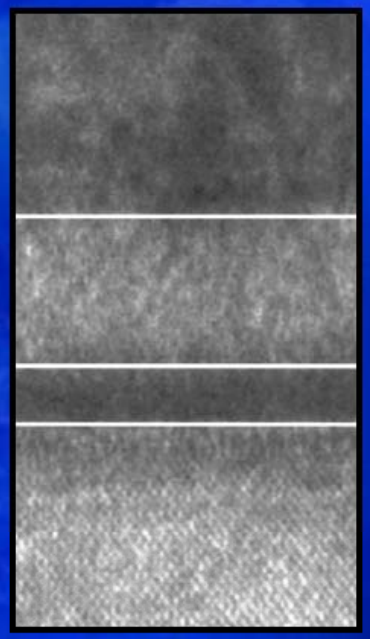


	90nm process	Experimental high-k
Capacitance	1X	1.6X
Leakage	1X	< 0.01X

Source: Intel

High-k + Metal Gate Transistors

- ✓ Integrated 45 nm CMOS process
- ✓ High performance
- ✓ Low leakage
- ✓ Meets reliability requirements
- ✓ Manufacturable in high volume



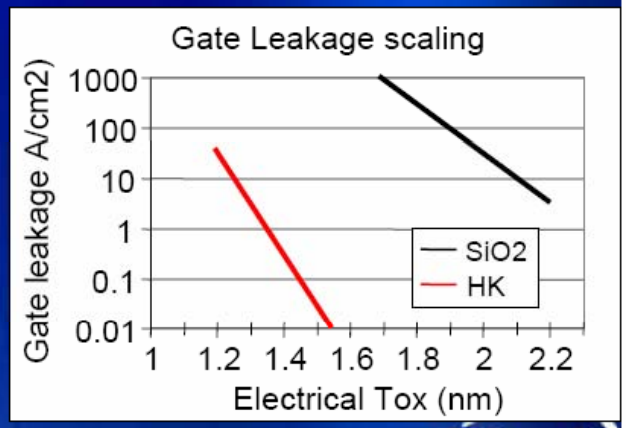
Low Resistance Layer

Work Function Metal
Different for NMOS and PMOS

High-k Dielectric
Hafnium based

Silicon Substrate

	High-k vs. SiO_2	Benefit
Capacitance	60% greater	*Faster transistors*
Gate Leakage	>100x reduction	*Cooler chips*



12th EMEA Academic Forum

EMEA ACADEMIC

hafnium silicate,
zirconium silicate,
hafnium dioxide
zirconium dioxide
HfSiON

J. Maiz,
Intel, 2007

Requirements of a new dielectric: Material

- Good stoichiometry (*i.e.* no vacancies and/or other defects)
- Structure (amorphous vs. crystalline)
- Uniform continuous films; small roughness
- Minimal thickness of interfacial layer(s)
- Thermal stability with respect to silicon
  - Subsequent to annealing at temperatures up to 1000ºC
- Low concentration of impurities (C, H, metals, *etc.*)

Source: Barry O'Sullivan (High-K group, Tyndall)

Requirements of a new gate dielectric

Processing and Integration Issues

- Compatibility with polysilicon processing (or metal gates)
- Diffusion barriers to dopants
- No metal diffusion into the Si channel
- Manufacturability (tools, *etc.)*
- Stability in air / water solubility ?

Source: Barry O'Sullivan (High-K group, Tyndall)

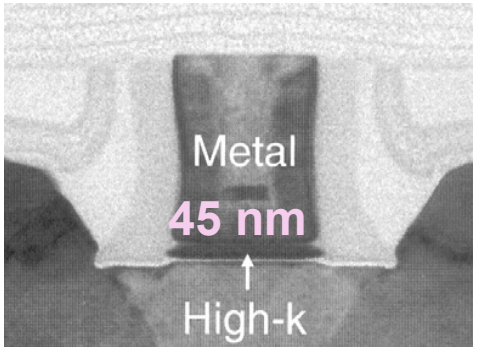
Requirements of a new dielectric : Electrical

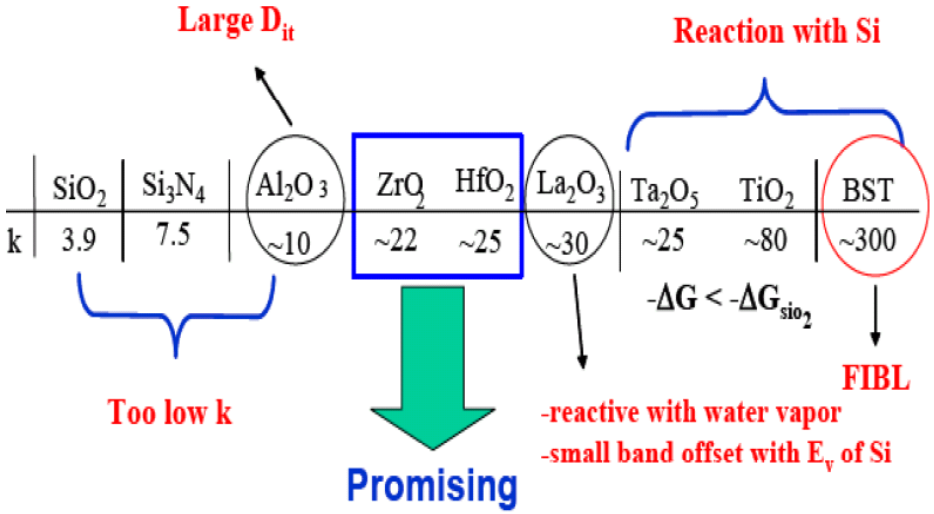
- High dielectric constant ($10 < \kappa < 50$)
- Low leakage current density (< 1 A cm^{-2} at $V_{GS} = V_{DD}$)
- Equivalent oxide thickness (T_{eq}) less than 1.2 nm
- Large band gap (> 6 eV) / suitable band offsets (> 1 eV)
- Electron / hole mobility ~ 95% SiO_2 / Si devices at 1 MV / cm
- Low concentration of bulk traps / fixed charge; no hysteresis
  - Small ΔV_{FB} shifts (cf. ideal)
- Reliability comparable to SiO_2
- Low interface state density, ~ mid 10^{10} cm^{-2} eV^{-1}

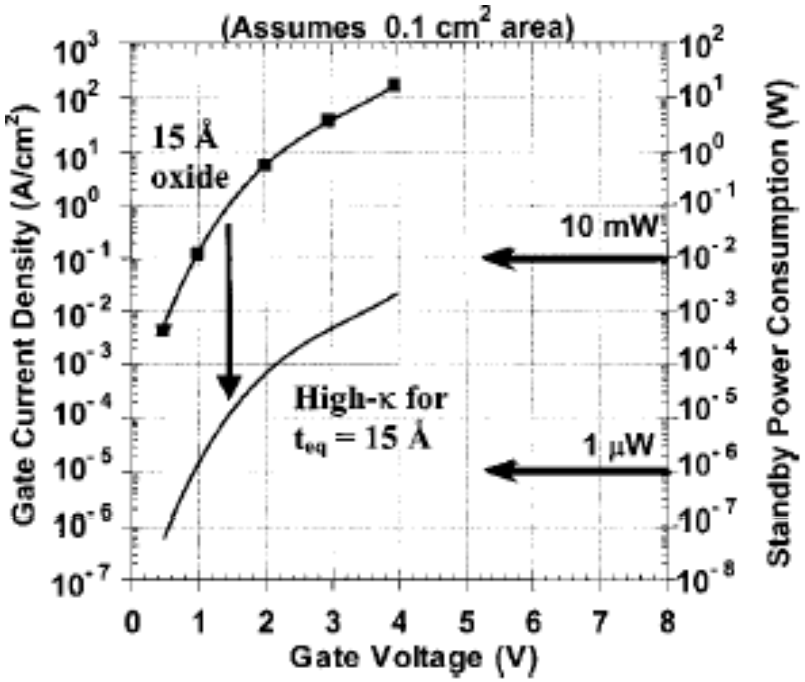
Source: Barry O'Sullivan (High-K group, Tyndall)

High-k Materials

- **Gate dielectric, silicon dioxide, is only a few atomic layers thick now ➔ leakage current increases**



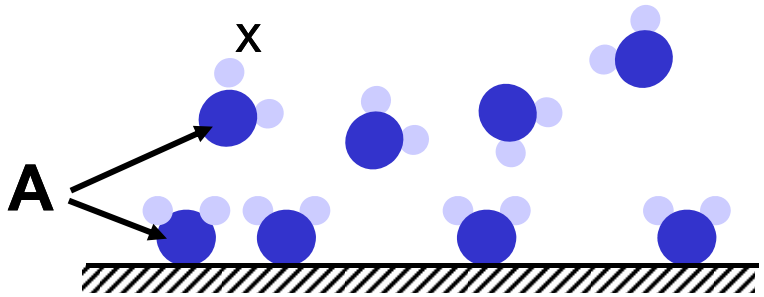




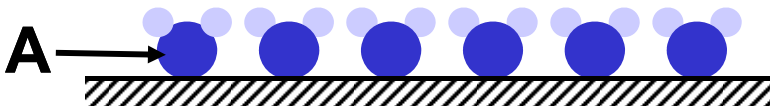
Huff et. al., Microelectronic Engineering, 69 (2003)

[J. Appl. Phys., 73 (1993) & 15 (2000), 83 (1998)]

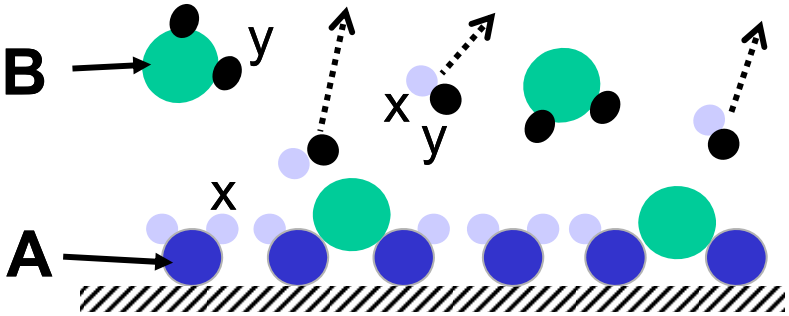
Crafting Films with Atomic Layer Deposition



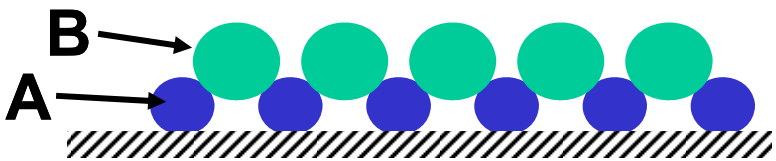
Step 1



Step 2

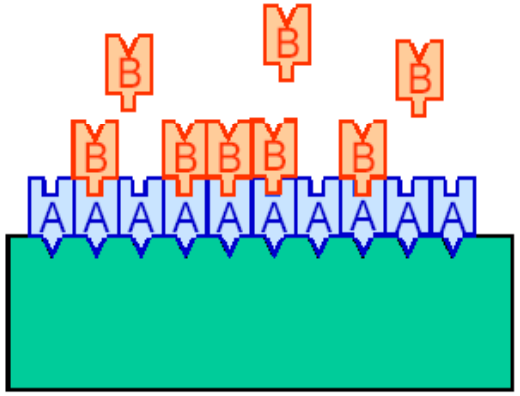


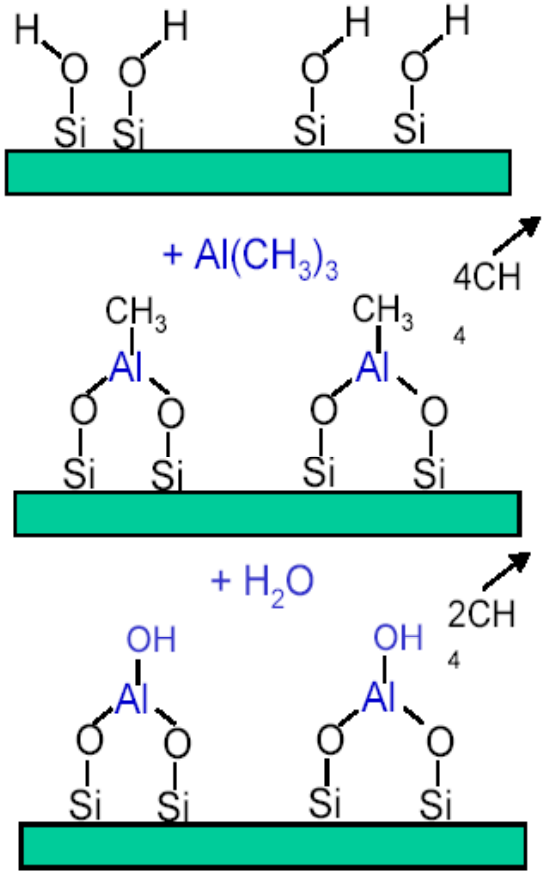
Step 3



Step 4

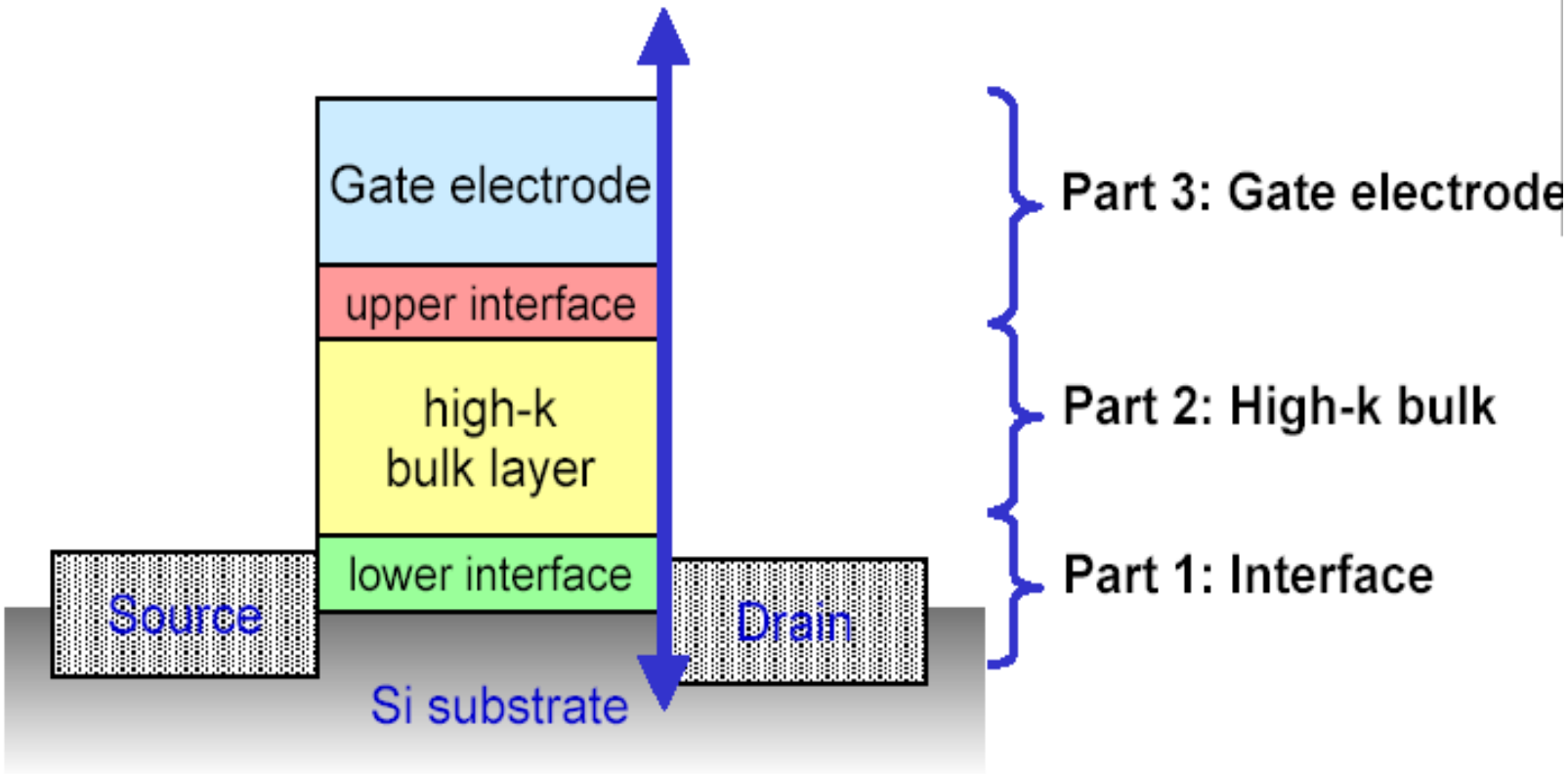
Atomic Layer Deposition (ALD) of Al_2O_3





- two self-limiting surface reactions are used in sequence to grow thin film
- ALCVD should result in good uniformity and thickness control
- chemical condition of starting surface is extremely important

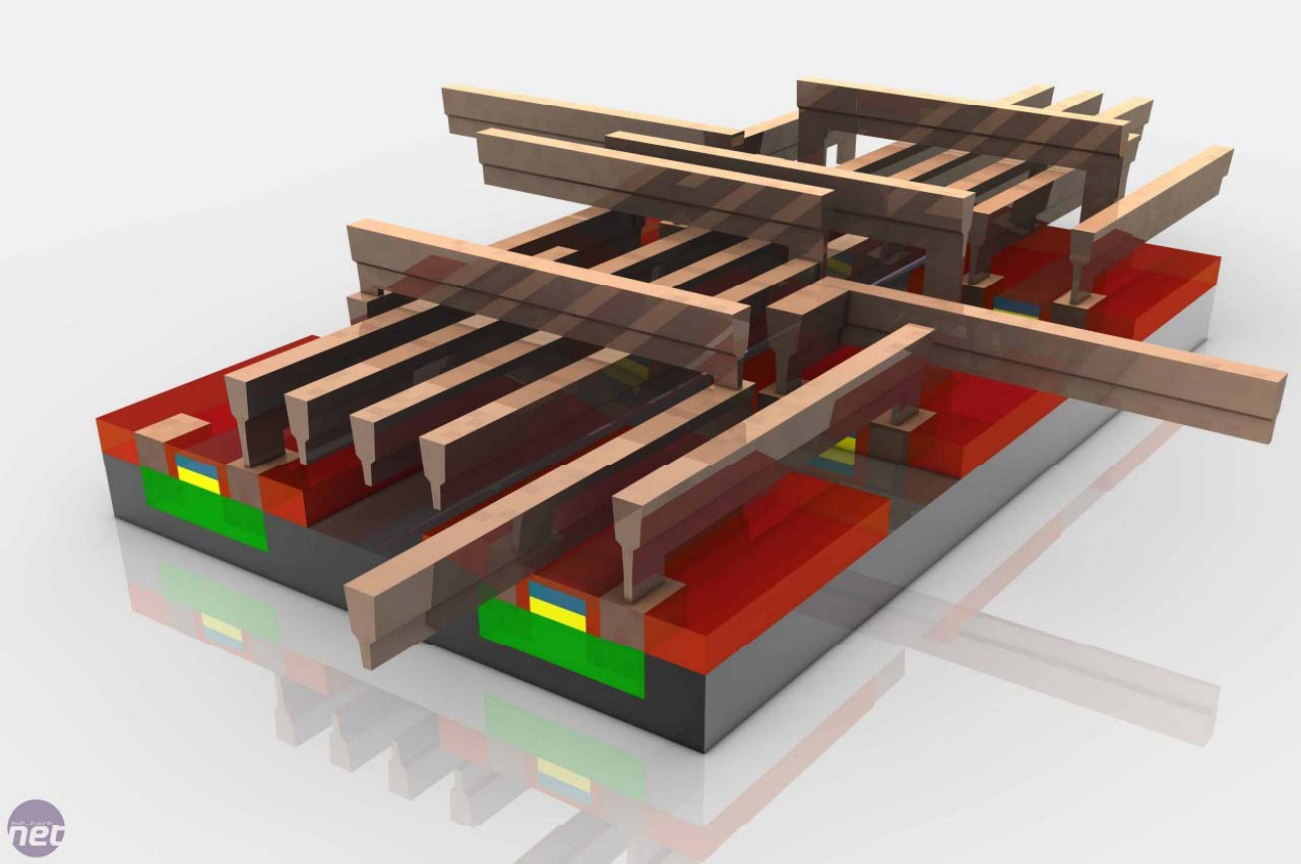
Current Gate Stack (based on HfO_2 high-K)



High K Gate

- Control Interface, Stress, Fixed charge, etc.
  - New additives?
- New Chemical Precursors
- New Gate Electrode Material
- New Etch Chemistries
- Future: Need K ~50-100

Interconnects



https://www.bit-tech.net/hardware/cpus/2010/06/10/how-to-make-a-cpu-from-sand-to-shelf/3

SHORT HISTORY OF INTERCONNECTS

1. Noyce Invention 1959
   Al & SiO2

2. Mid 1970's
   Sputtered Al Alloys
   Deposited SiO2

3. Late 70's
   Dry Etch, 2 Level Metal

4. Early 80's
   W @ M1, W Plugs
   ≤ 2 Level metal; SiO2, Al Alloys

5. Late 80's
   CMP
   < 2 Level metal; SiO2, Al Alloys

Early 90's Interconnect becomes a performance limiter

6. 1997 IBM Announces Cu
   Damascene Cu & SiO2

7. Late 90's early 2000s
   Florosilicate Glass K~3.5+

8. NOW
   Silk, OSG K~2.8

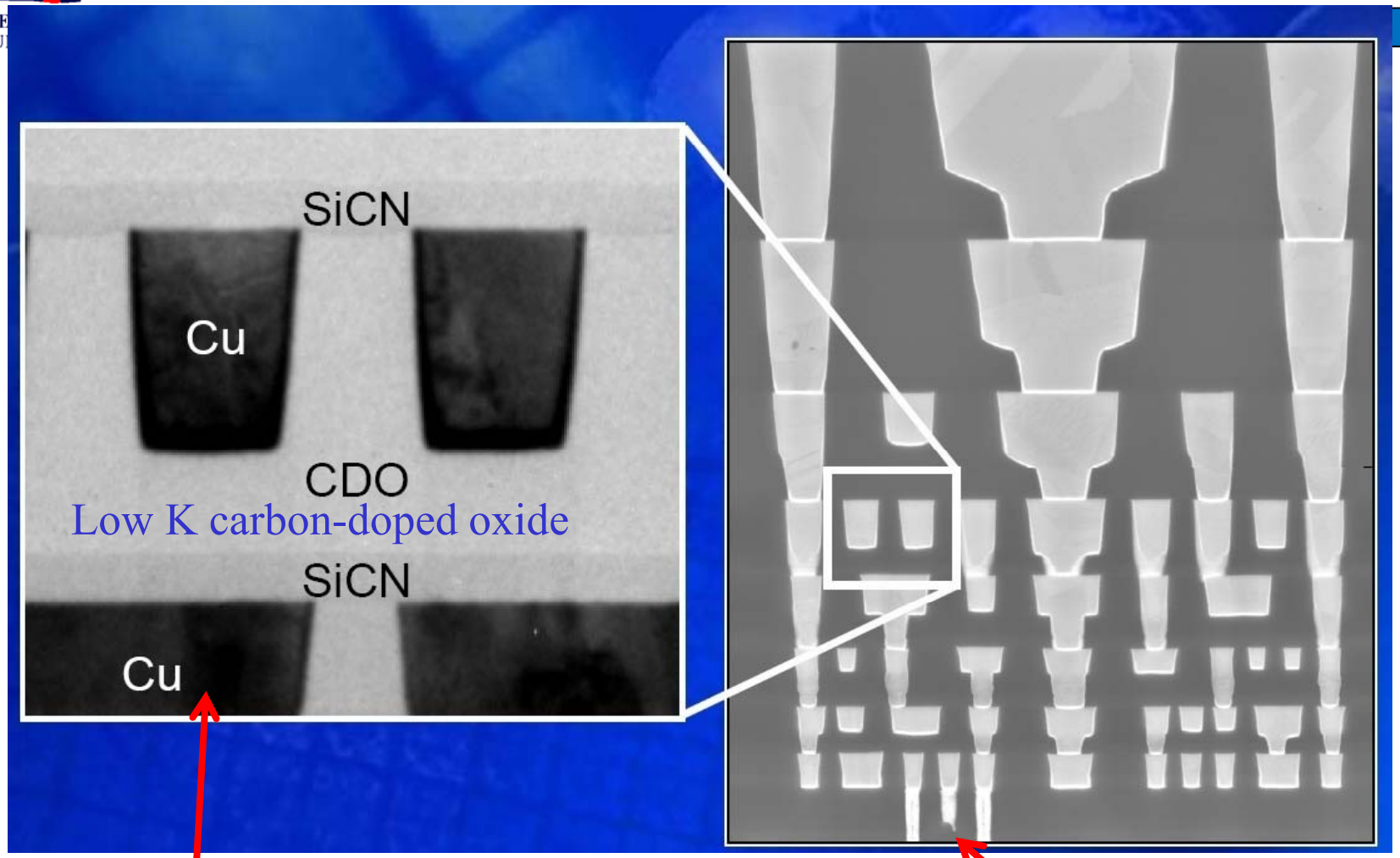
9. 2007 *K=2.7-2.4*
10. 2010 *K=2.1*
11. 2013 *K=1.9*

5 Changes, 1st 35 Years; Planning 6 Changes, 16 Years; then No More "Materials Solutions"

Source: K. Monnig, SEMATECH

Interconnect Material Challenges at 65 nm node

8 layers of metal



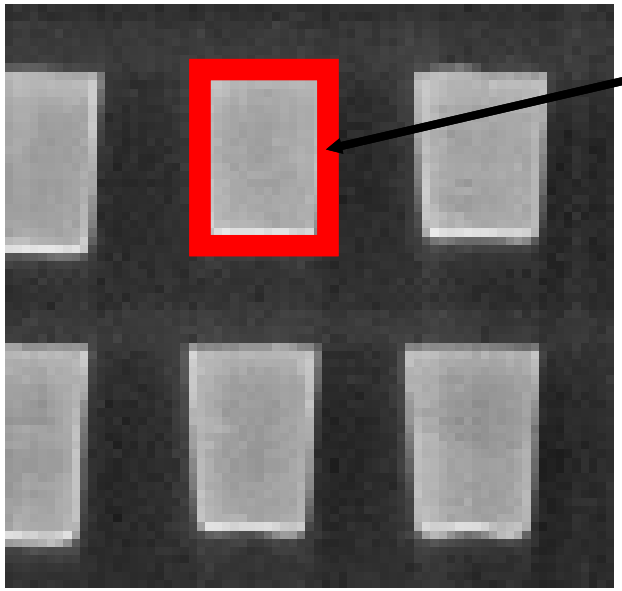
Copper interconnects

Device

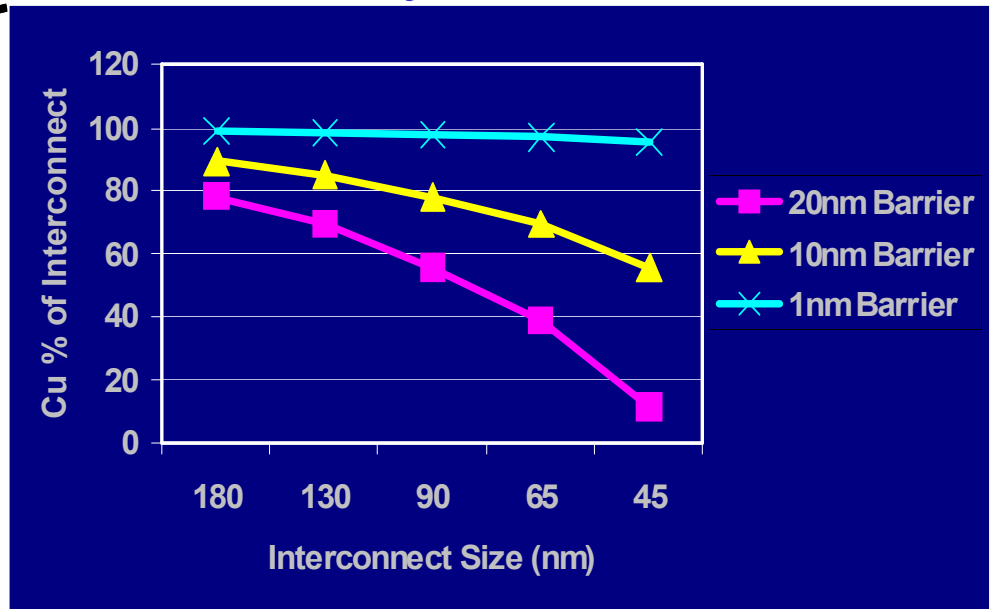
Two-layer dielectric for low capacitance and low cost.
Must Reduce Dielectric Constant (K) and Resistance

J. Maiz, Intel, 2007

Interconnect Resistance: Barrier Layers



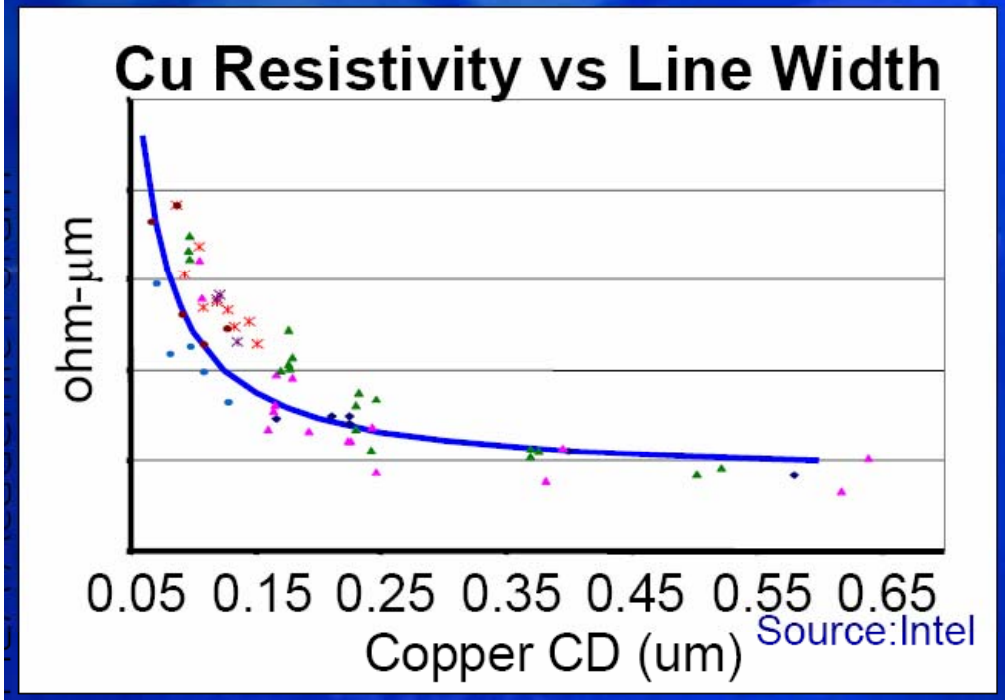
~ 20 nm barrier layer

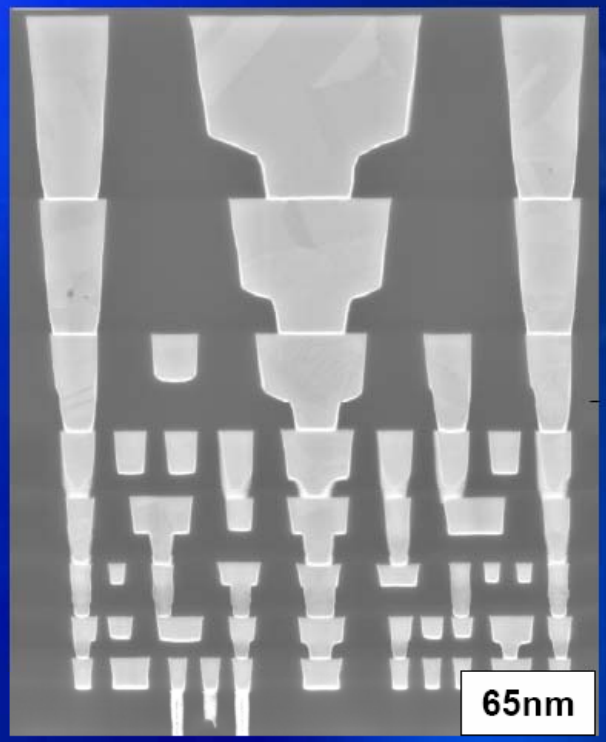


- Need thin but effective barrier to prevent Cu diffusion
- Would prefer Self Assembling Precursors vs deposition
- Need Adhesion to all layers
- New material &/or deposition technology…

Interconnect Resistance: Increased Resistivity

- Need thin but effective barrier to prevent Cu diffusion
- Would prefer Self Assembling Precursors vs deposition
- Need Adhesion to all layers
- New material &/or deposition technology…





- **Effective resistivity increase due to:**
  - Cross section reduction due to barriers
  - Increased scattering from grain boundaries and surfaces

Low-*K materials for high speed gates*

SiO_2 has a relative dielectric constant

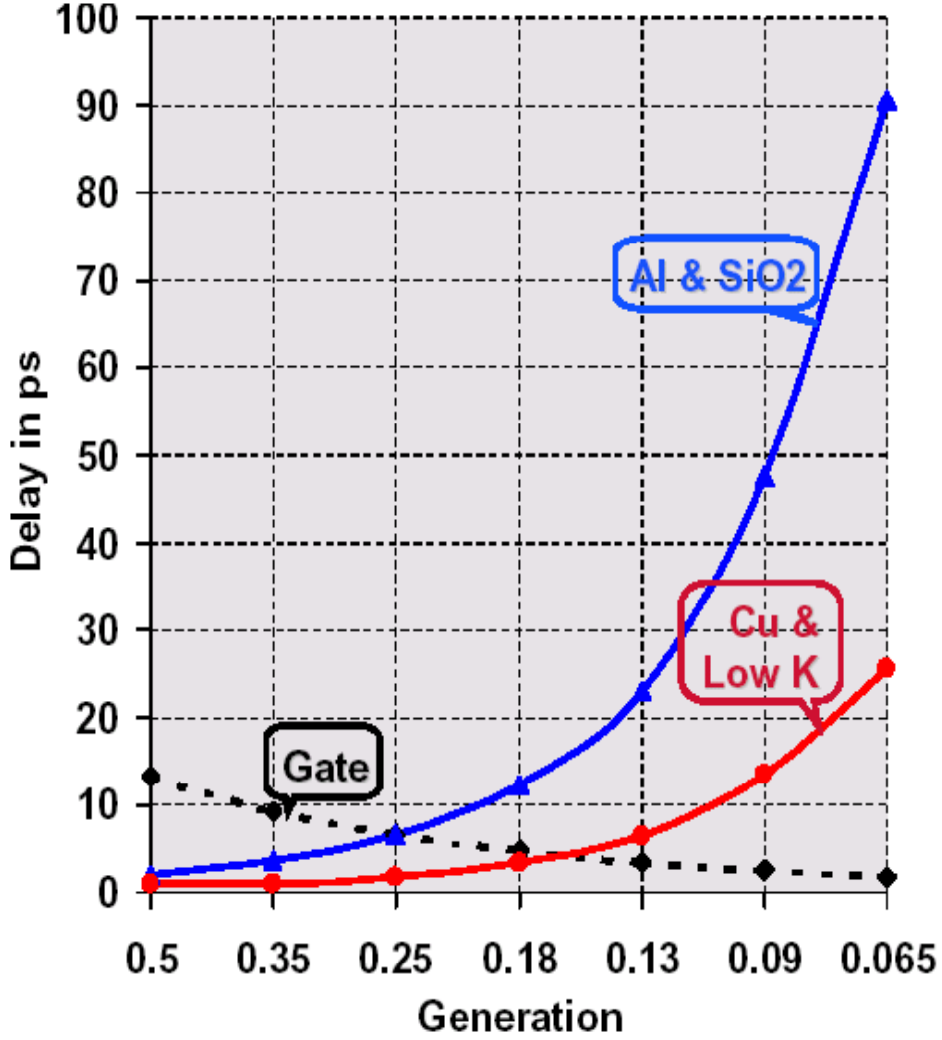
$$K = \varepsilon_r = \frac{\varepsilon}{\varepsilon_0} = 3.9$$

Low-k materials those that have dielectric constant smaller than SiO_2.
(i.e. K= 3.7 for SiCN, K= 3.0 for C:SiO_2)
Dielectric constant influences in the capacitance of the gate and thus, it may limit its response time

$$C = \frac{S K \varepsilon_0}{d} \qquad \tau = RC$$

Low-*K materials for high speed gates*

SPEED / PERFORMANCE ISSUE — *The Technical Problem*



- Gate Delay
- Interconnect Delay, Al & SiO2
- Interconnect Delay, Cu & Low K

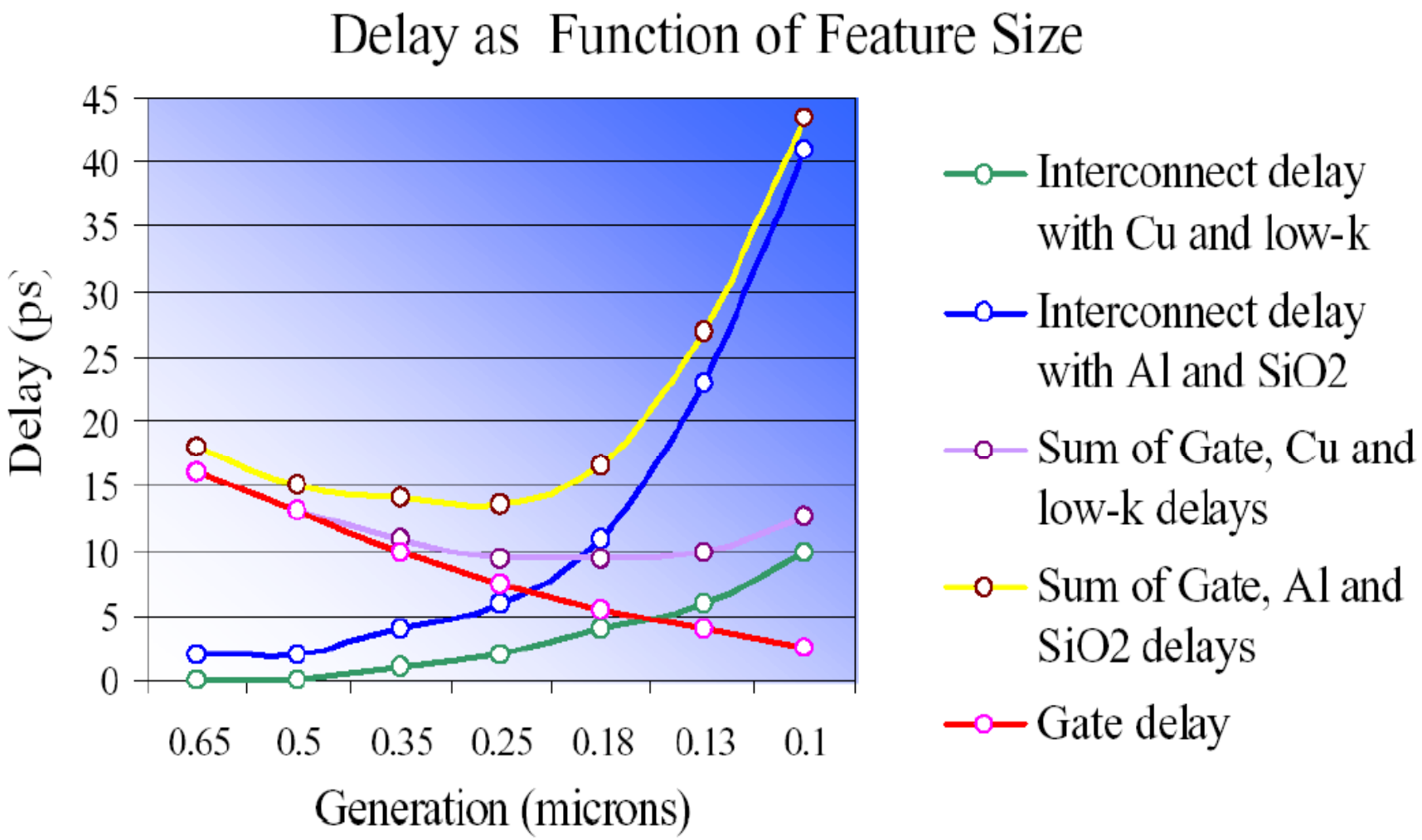
Interconnect will dominate timing delay.

Cu/Low-k buys 1-2 generations.

Al	*3.0 uΩ-cm*
Cu	*1.7 uΩ-cm*
SiO2,	*K=4.0*
Low K	*K=2.0*
Al & Cu	*.8u Thick*
Al & Cu Line	*436u Long*

Data From: Bohr, Mark T; "Interconnect Scaling - The Real Limiter to High Performance ULSI"; Proceedings of the 1995, IEEE International Electron Devices Meeting; pp241-242

Source: K. Monnig, SEMATECH


Delay as Function of Feature Size
Delay (ps)
45
40
35
30
25
20
15
10
5
0
0.65
0.5
0.35
0.25
0.18
0.13
0.1
Generation (microns)
Interconnect delay with Cu and low-k
Interconnect delay with Al and SiO2
Sum of Gate, Cu and low-k delays
Sum of Gate, Al and SiO2 delays
Gate delay

UNIVERSITAT JAUME·I

The Previous Model is Simplistic But…….

- Not all Products/Circuits are RC Delay Limited
- Some Cross Talk Limited (line-line C)
- 30%-70% Power Dissipated in Interconnects (R, C indirectly)
- Reliability (Copper helps, Low-K doesn't)

SO

Becoming Clear That TEM Mode Wires Wrapped in Insulators are Becoming a Performance Limiter.

&

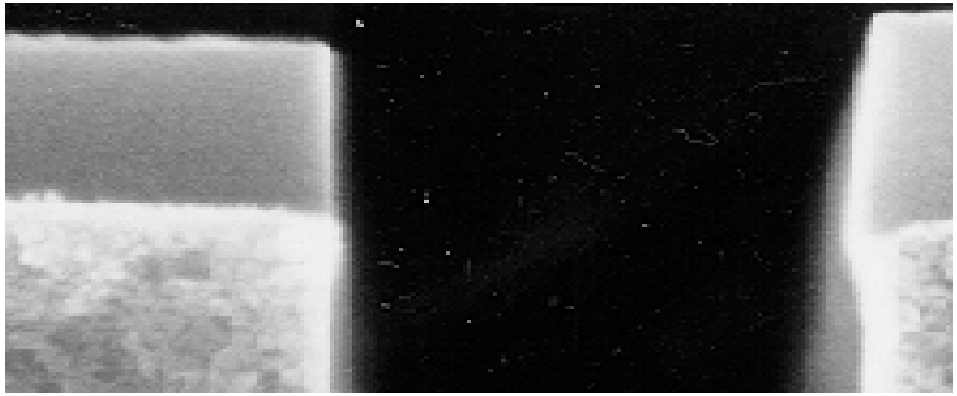
Unlike Almost Everything Else in IC technology "Shrinks" Degrade Interconnect Performance

INTERNATIONAL SEMATECH · SEMATECH

Source: K. Monnig, SEMATECH

Super Materials Needed for low-*K*

- Stress in process & assembly a big issue
- Design Electrical & Mechanical Properties
- Improve adhesion between materials
- Molecular self assembly…
- Nano-materials

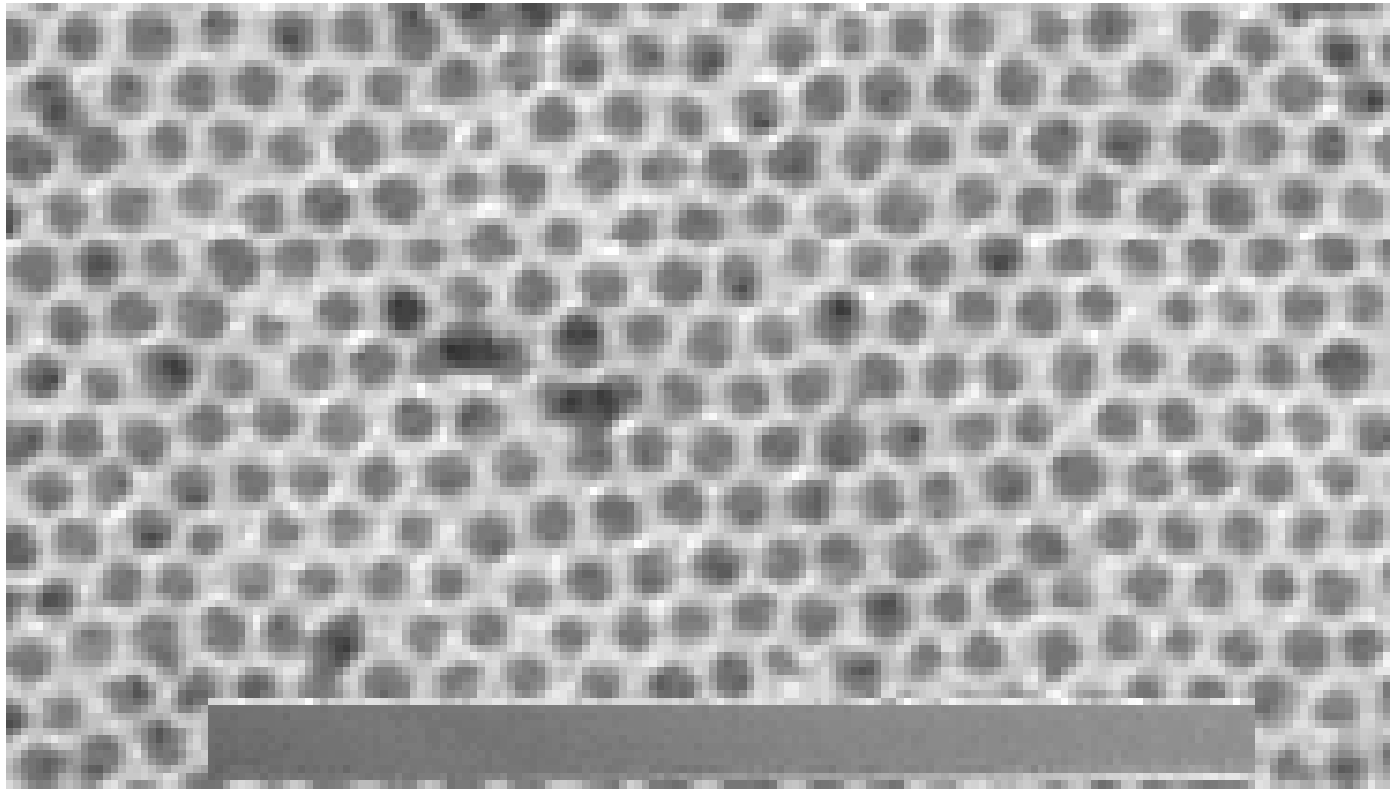


Source: Intel

Low-k xerogel structure

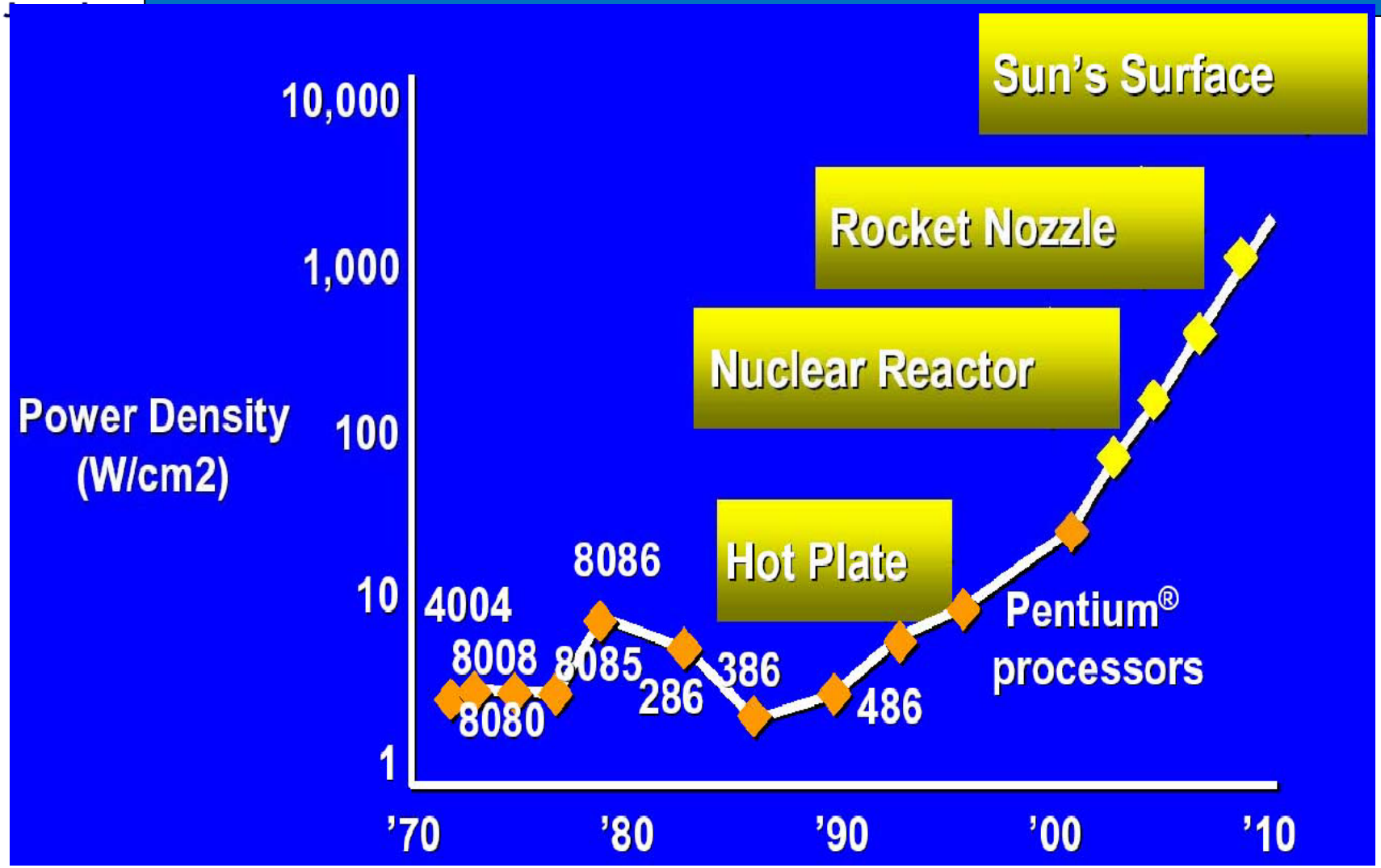
Mechanical Strength and Integration Issues

Self Assembled Nanoporous Low K Dielectric



(M.A. Morris, Chemistry Dept., UCC)

Power Dissipation – Key Challenge (old graphic)



Intel

Silicon Scaling Summary

- Scaling continues …….
- Lithography: New tools and processes needed
- Many new materials needed
  - Lithography
  - Transistor
  - Interconnects
  - Molecular assembly….
- Lower K ILDs are weaker
  - Mechanical issues in processing
  - Mechanical issues in assembly

Dynamic Power Dissipation

→ Scaling Supply Voltage (V_{DD})

$$P_{dynamic} = C_{load} \cdot V_{DD}^2 \cdot f$$

$$I_d = \mu \cdot C_{ox} \cdot (W/L) \cdot (V_g - V_T) \cdot V_{ds} \qquad (@V_{ds} = V_{DD})$$

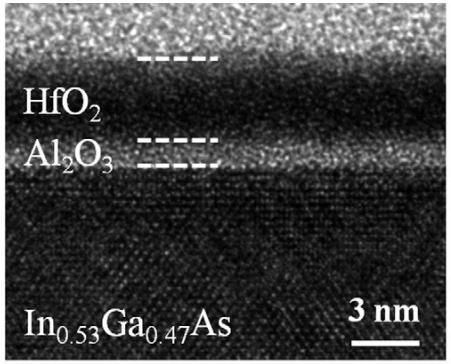
Introduce high mobility materials to reduce V_{DD}

Material	Si	Ge	GaAs	$In_{0.53}Ga_{0.47}As$	InAs	InSb
Electron Mobility (cm^2/Vs)	1400	3900	8500	14000	40000	78000
Hole mobility (cm^2/Vs)	450	1900	400	300	500	850

Challenges for III-V MOSFETs

Integration of High-*k* on III-V

$HfO_2/Al_2O_3/InGaAs$



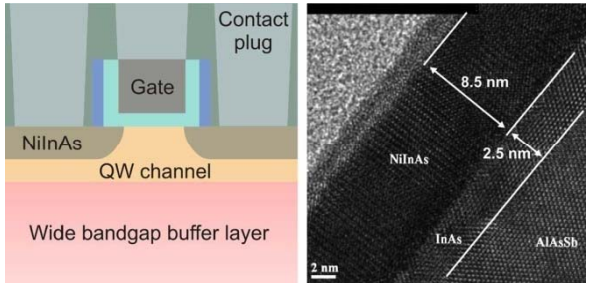
Chu, *APL*, 99:4, 042908 (2011)

Control of oxide/InGaAs interface

Target:
SS ~ 60 mV/dec.

Scaling (S/D Resistance)

"Nikelide" Phase

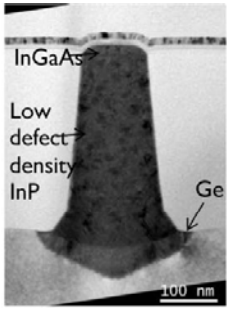


Oxland, IEEE *EDL*, 33:4, 501 (2012)

Target for 12-nm node:
$\rho_C = 5 \times 10^{-9}\ \Omega.cm^2$

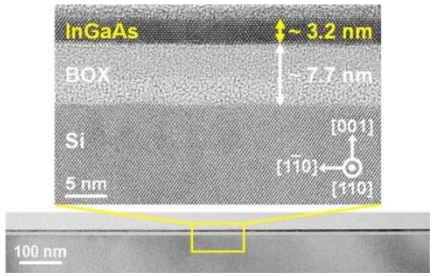
Integration of III-V on Si

Aspect Ratio Trapping



Waldron, *ECST*, 45:4, 115 (2012)

Bonding



Yokoyama, IEEE *EDL*, 32:9, 1218 (2011)

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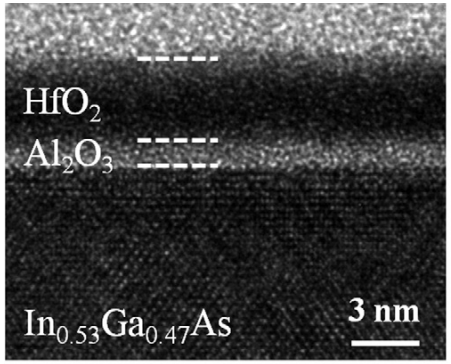
Challenges for III-V MOSFETs

Integration of High-*k* on III-V

$HfO_2/Al_2O_3/InGaAs$



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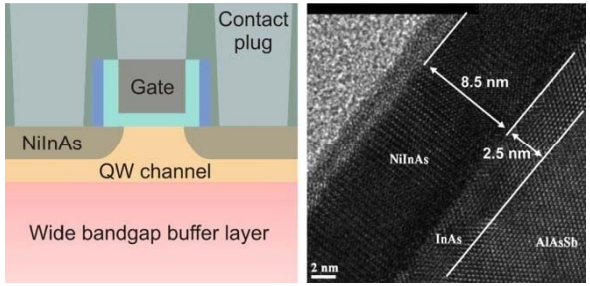

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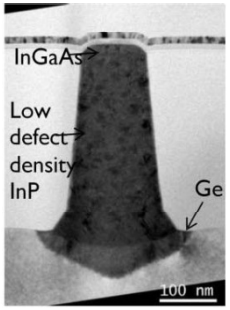

Waldron, *ECST*, 45:4, 115 (2012)

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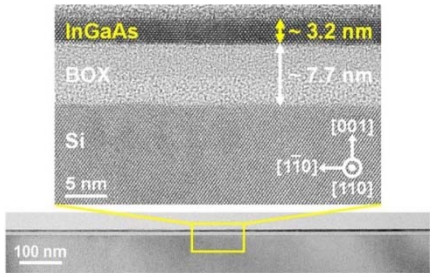

Yokoyama, IEEE *EDL*, 32:9, 1218 (2011)

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